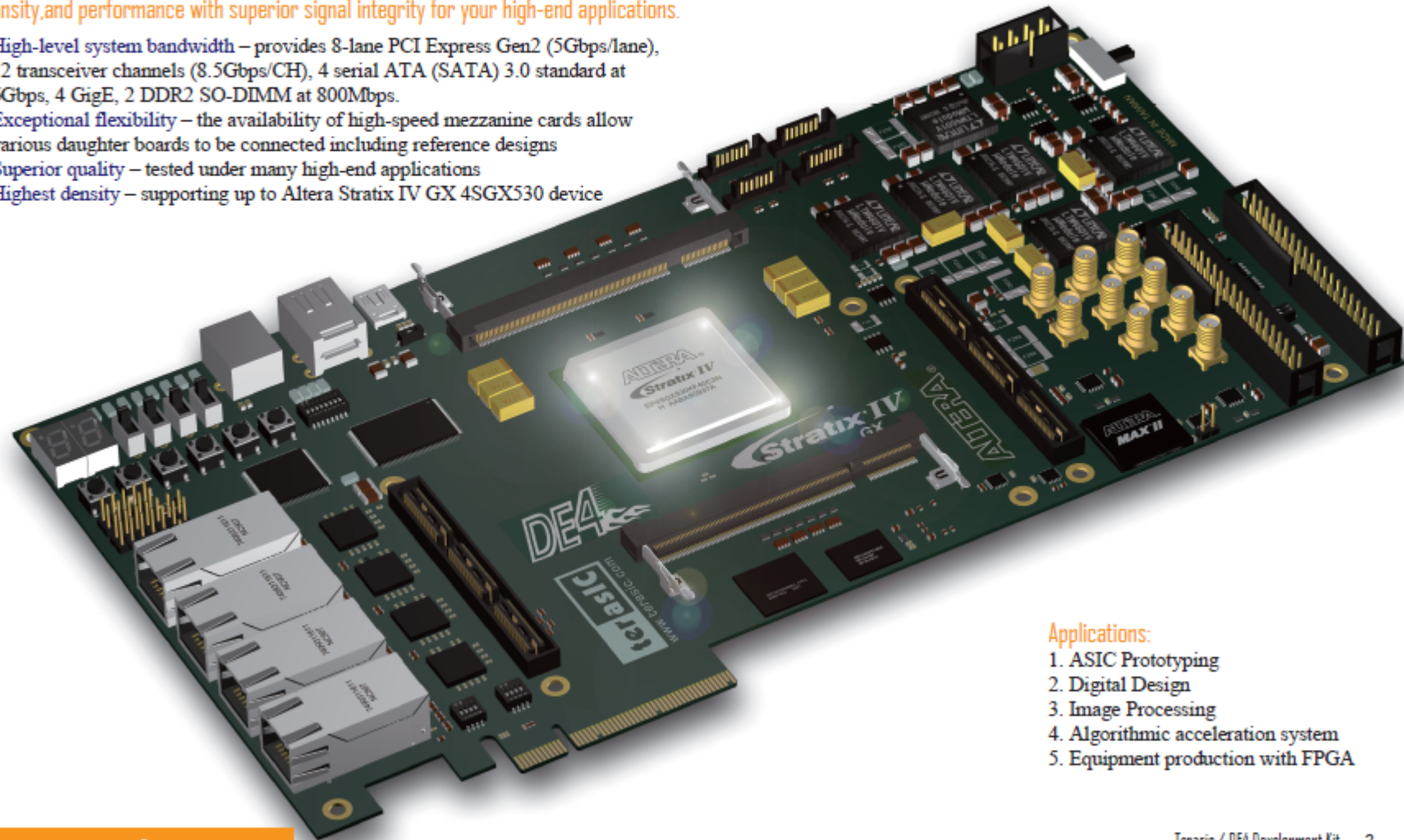


立野電腦（株）は、Altera Stratix IV 搭載の DE4-530/230, ProceIV-360/530/820, ProcStarIV-530/820, Proc_SoCを出荷中。

The DE4 Stratix IV GX FPGA board delivers unprecedented level of system bandwidth, density, and performance with superior signal integrity for your high-end applications.

- **High-level system bandwidth** – provides 8-lane PCI Express Gen2 (5Gbps/lane), 12 transceiver channels (8.5Gbps/CH), 4 serial ATA (SATA) 3.0 standard at 6Gbps, 4 GigE, 2 DDR2 SO-DIMM at 800Mbps.
- **Exceptional flexibility** – the availability of high-speed mezzanine cards allow various daughter boards to be connected including reference designs
- **Superior quality** – tested under many high-end applications
- **Highest density** – supporting up to Altera Stratix IV GX 4SGX530 device



Applications:

1. ASIC Prototyping
2. Digital Design
3. Image Processing
4. Algorithmic acceleration system
5. Equipment production with FPGA

www.terasic.com

Terasic / DE4 Development Kit 2

DE4資料 正規代理店 立野電腦（株） <http://www.dsp-tdi.com>

Introduction

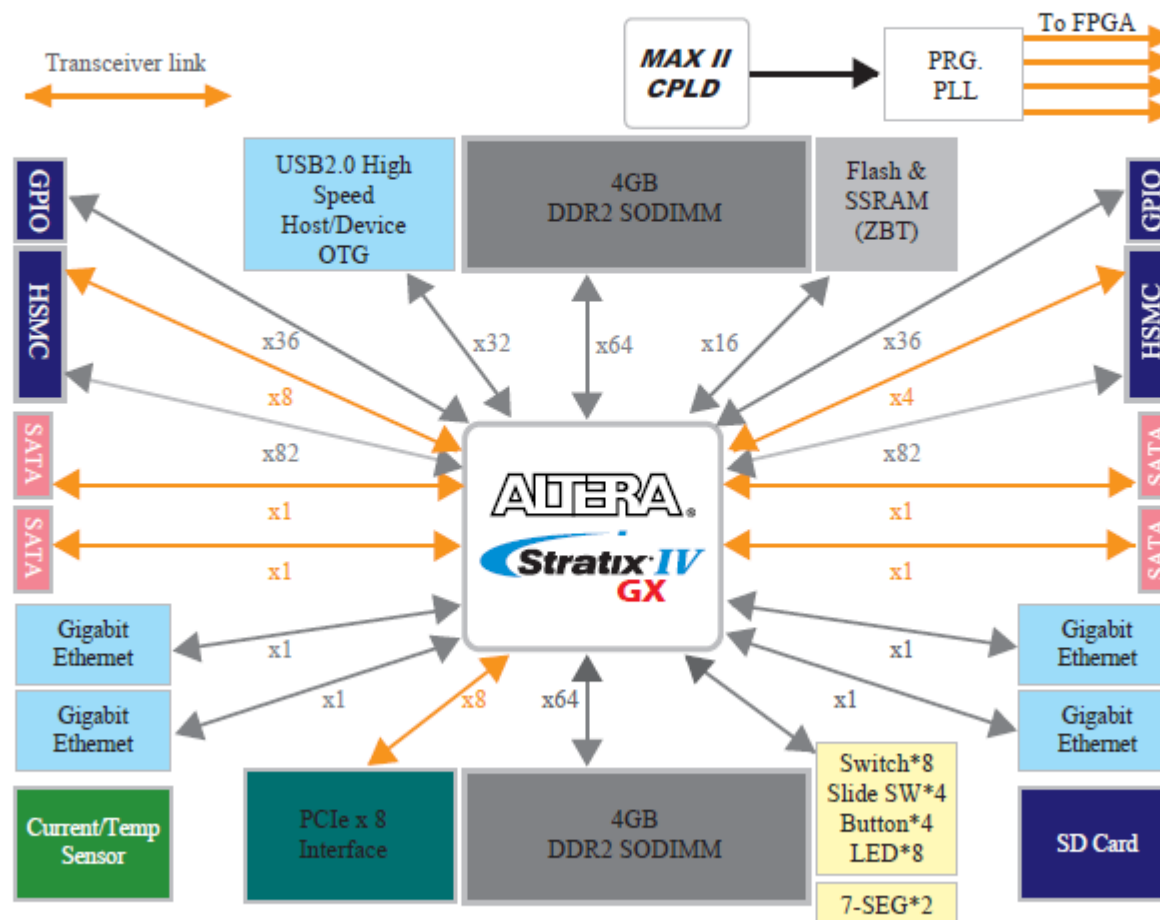


Terasic announces the availability of its latest DE4 development board targeting Stratix IV GX FPGA. Leveraging on the success of the DE series, the DE4 development board provides the ideal hardware platform for developing and prototyping low-power, high-performance, and high density designs. Powered by the Stratix® IV GX device and supported by industry-standard peripherals, connectors and interfaces, the DE4 board offers a rich set of features that is suitable for a wide range of compute-intensive applications.

The advantages of the Stratix® IV GX FPGA platform with embedded transceivers has allowed the DE4 board to fully compliant with version 2.0 of the PCI Express standard. Additionally, has allowed the DE4 board to support serial ATA (SATA) interfaces making it possible to leverage the integration option for storage applications.

Two High-Speed Mezzanine Card (HSMC) connectors are available to provide additional functionality and connectivity via HSMC daughter boards and cables. For large-scale ASIC prototype development, it can be established by a cable connecting to multiple DE4/FPGA boards through the DE4 connector interfaces.

Block Diagram



Features



The DE4 board comes in two available FPGA devices:

- **EP4SGX230**

- 228,000 logic elements (LEs)
- 17,133K total memory bits
- 1,288 18x18-bit multipliers blocks
- 2 PCI Express hard IP blocks
- 744 user I/Os
- 8 phase locked loops (PLLs)

- **EP4SGX530**

- 531,200 logic elements (LEs)
- 27,376K total memory bits
- 1,024 18x18-bit multipliers blocks
- 4 PCI Express hard IP Blocks
- 744 user I/Os
- 8 phase locked loops (PLLs)



Configuration device and USB Blaster circuit

- MAXII CPLD EPM2210 System Controller and Flash Fast Passive Parallel (FPP) configuration
- On-board USB Blaster for use with the Quartus II Programmer
- Programmable PLL timing chip configured via MAX II CPLD / FPGA
- Support JTAG mode



Memory devices

- 512-Mb Flash (32M x 16) with a 16-bit data bus
- 16-Mb SSRAM (1M x 16)

Features



Two DDR2 SO-DIMM sockets

- Up to 8-GB capacity in total
- Run at 400 MHz



Push-button switches

- 4 user-defined inputs
- Low active



Slide switches

- 4 slide switches for user-defined inputs



On-Board Clocking Circuitry

- 50MHz/100MHz oscillator
- 2 SMA connector for external transceiver clock input
- 4 SMA connector for LVDS clock input/output
- 2 SMA connectors for clock output
- 1 SMA connector for external clock input



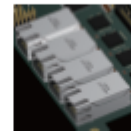
SD card socket

- Provides SPI and 4-bit SD mode for SD Card access



Four Serial ATA ports

- Support SATA 3.0 standard 6Gbps signaling rate



Four Gigabit Ethernet ports

- Integrated 10/100/1000 Gigabit Ethernet Transceiver
- Support Power Over Ethernet (POE) optional



PCI Express x8 edge connector

- Support connection speed of Gen1 at 2.5Gbps/lane to Gen2 at 5.0Gbps/lane
- Connection established with PC motherboard with x8 or x16 PCI Express slot

Features



Two 172-pins High Speed Mezzanine Card (HSMC)

- 2 female-HSMC connectors include 8.5Gbps transceivers x12
- I/O voltage 2.5V



Two 40-pin expansion headers

- 72 FPGA I/O pins
- 40-pin header is designed to accept a standard 40-pin ribbon cable for external connection
- Compatible with I/O standard 3.3V



USB Host/Slave controller

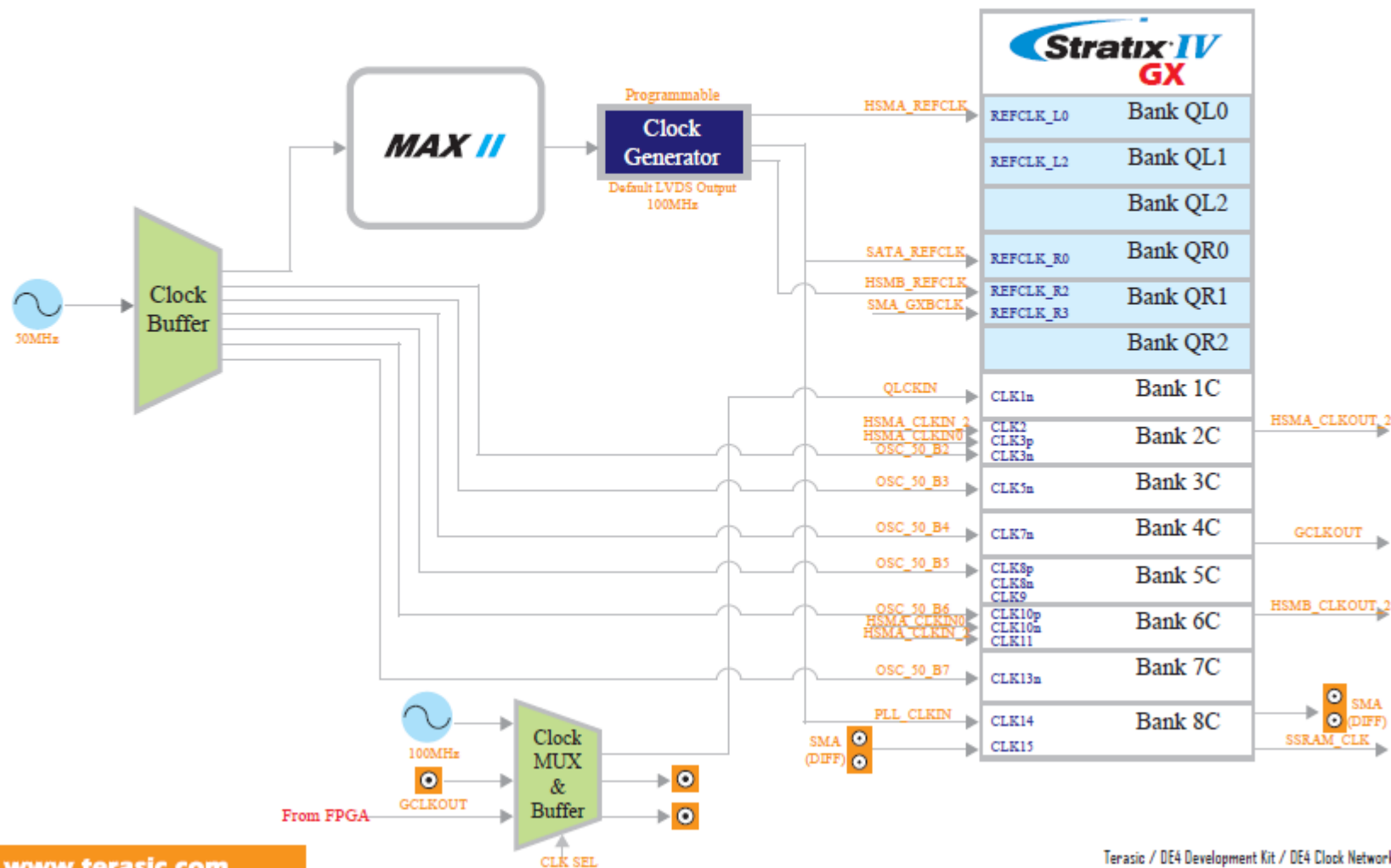
- Complies fully with USB 2.0
- Support data transfer at high-speed, full-speed, and low-speed
- Support both USB host and device
- Three USB ports (one type mini-AB for host/device and two type A for host)
- Support Nios II with the Terasic driver



Power

- Stand alone DC input 12V and 3.3V
- PCI Express edge connector power

DE4 Clock Network



Ordering Product Name & Specifications

Ordering Product Name	DE4-230	DE4-530
FPGA Device	EP4SGX230KF40C2	EP4SGX530KH40C2
FPGA Logic Elements(LEs)	228,000	531,200
Serial ATA	4 (6Gbps)	4 (6Gbps)
SSRAM(ZBT)	16 Mb	16 Mb
FLASH	512 Mb	512 Mb
DDR2 SO-DIMM Socket	2 (400MHz)	2 (400MHz)
SD Card Socket	Yes	Yes
EEPROM	Yes	Yes
Temp Sensor	Yes	Yes
Power Monitor	Yes	Yes
USB Blaster	Built-in	Built-in
USB 2.0 OTG	Yes (High Speed)	Yes (High Speed)
PCI Express x8	Yes (Gen2)	Yes (Gen2)
Gigabit Ethernet (10/100/1000)	4	4
HSMC	2 (Includes 8.5Gbps Transceiver)	2 (Includes 8.5Gbps Transceiver)
40-pin GPIO	2	2
LEDs	8	8
Slide Switches	4	4
Push Buttons	4	4
Seven Segment	2	2
SMA Connector	9	9
Demo Source Code	Included	Included

立野電脳（株）は、Altera Stratix IV 搭載の DE4-530/230, ProceIV-360/530/820, ProcStarIV-530/820, Proc_SoCを出荷中。

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必ず事前にお問い合わせと見積書をご請求ください。DE4は研究開発用です。
最終製品に組み込んでの利用は、想定されていません。
製品詳細資料をメーカーwebからdownloadしてご検討ください。



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