FPGAボードで画期的なGUIを創造しませんか。
マルチタッチパネル、5Mピクセルカメラを備えたVEEK-MTは立野電脳（株）が供給するTerasic Technologies社の 2012年 最新 FPGA開発キット。従来のAudio,Video(in),VGA(out),LAN(dual Gbit),USB,SDcard,RS232C I/Fも利用可能。

型番 VEEK-MT お問い合わせはsales@dsp-tdi.com

Contents

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1 Overview

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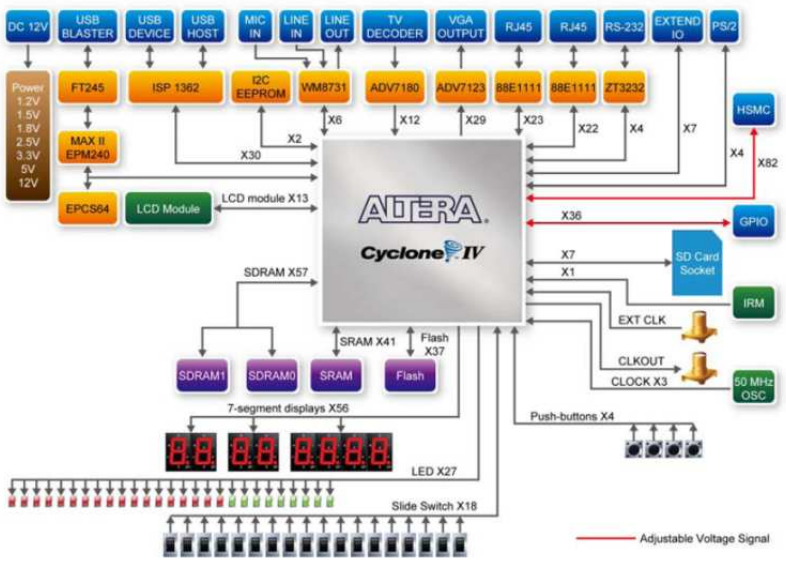
Specifications

1. Altera Cyclone IV E - EP4CE115F29
2. USB Blaster for Programming
3. SDRAM/SRAM/FLASH/SD-Card
4. Extensive Multimedia Support
5. Abundant Communication Selection
6. 5 Megapixel Camera
7. 7” Capacitive Touch Screen

DE2-115 Block Diagram



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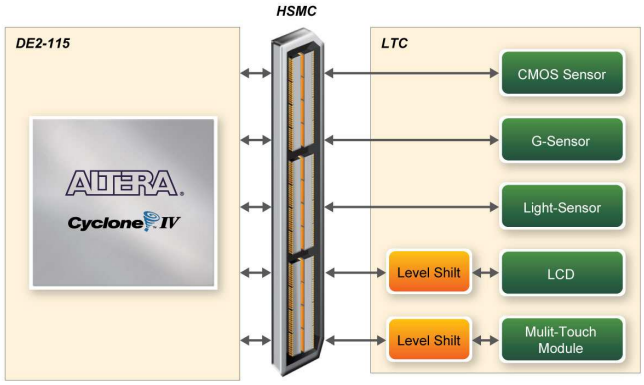
Touch Screen Module Block Diagram



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Top View

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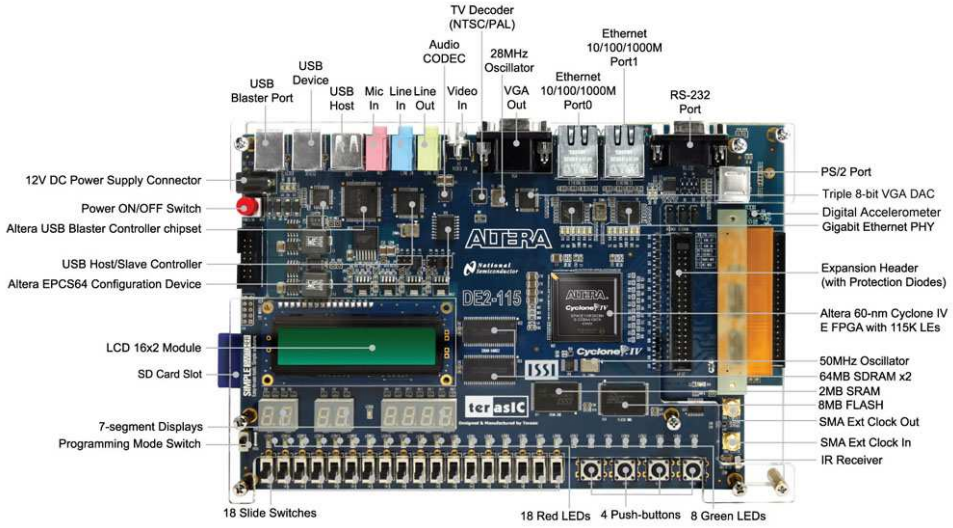
Back View



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2 Features

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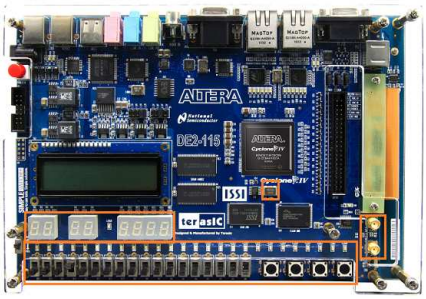
Basic I/O

- Three 50MHz oscillator clock inputs
- SMA connectors
- 16x2 LCD module
- 18 slide switches
- 4 Push-buttons
- 18 red and 9 green LEDs
- Eight 7-segment displays



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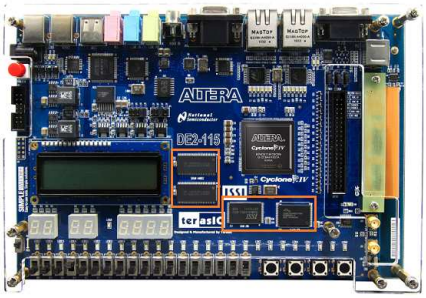
Memory

- 128MB (32Mx32bit) SDRAM
- 2MB (1Mx16) SRAM
- 8MB (4Mx16) Flash
- 32Kb EEPROM
- SD-Card Slot



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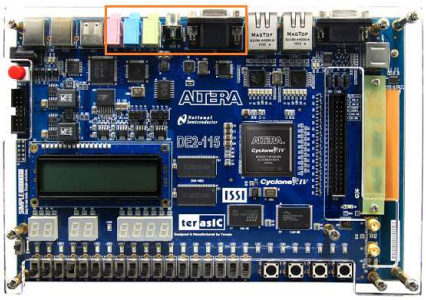
Multimedia

- 24-bit Audio Codec
  - Mic-in
  - Line-in
  - Line-out
- TV-in Analog Decoder
- 8-bit VGA Output



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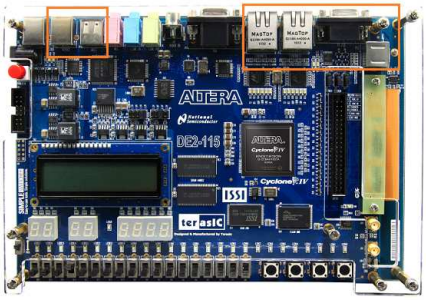
Communication

- USB Host/Device 2.0
- RS232 DB9 Connector
- 2 Gigabit Ethernet Ports
- Infrared Receiver
- PS/2 Port



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Screen Module Features

- 7” Capacitive Touch Screen
  - 24-bit RGB Interface
  - Supports multi-touch gesture and single-touch
- 5 Megapixel Digital Camera
- Ambient Light Sensor
- 3-axis Accelerometer

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3 Extension Ports

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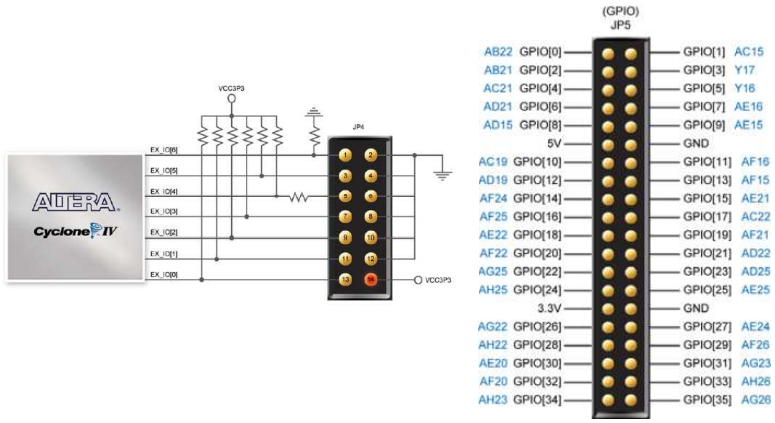
General Purpose Input Output

- 40 I/O connected to FPGA
- 14 I/O pins connected to FPGA



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4 Utilities

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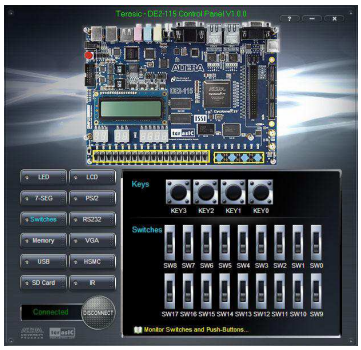
Control Panel Utility

The DE2-115 board comes with a PC-based Control Panel that allows users to access various components onboard. The host computer communicates with the board via USB port. The tool can be used to verify the functionality of components.



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System Builder

The DE2-115 System Builder is a Windows-based software utility, designed to assist users in creating a Quartus II project for the DE2-115 board within minutes. The generated Quartus II project files include:

- Quartus II Project File (.qpf)
- Quartus II Setting File (.qsf)
- Top-Level Design File (.v)
- External PLL Controller (.v)
- Synopsis Design Constraints file (.sdc)
- Pin Assignment Document (.htm)

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Application Selector

The application selector displays all of the FPGA configurations available on the inserted SD card according to a predefined format. Users are able to load different programs independent of a PC.

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5 Advanced Demonstrations

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Painter Demonstration

This demo shows how to control LCD and touch controller to establish a paint demo based on SOPC Builder and Altera VIP Suite. The demonstration shows how multi-touch gestures and single-touch coordinates operate.

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Picture Viewer

This demonstration shows a simple picture viewer implementation using Nios II based SOPC system. It reads JPEG images stored on SD Card and displays them on the LCD.

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Picture Viewer

The Video and Image Processing (VIP) Example Design demonstrates dynamic scaling and clipping of a standard definition video stream in either National Television System Committee (NTSC) or Phase Alternation Line (PAL) format and picture-in-picture mixing with a background layer. The video stream is output in high resolution (800×480) LCD touch panel.

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Camera Application

This demonstration shows a bubble level implementation based on a digital accelerometer. This design uses I^2C protocol to control the ADXL345 digital accelerometer, and the APDS-9300 Miniature Ambient Light Photo Sensor.

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Camera Application

This demonstration shows a digital camera reference design using the 5-Megapixel CMOS sensor and 8-inch LCD modules on the VEEK-MT. The CMOS sensor module sends the raw image data to FPGA on the DE2-115 board, the FPGA on the board handles image processing part and converts the data to RGB format to display on the LCD module.

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