Terasic Multimedia Touch Panel Daughter Board (MTDB)

User Manual

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Chapter 1
The Package

The Multimedia Touch Panel Daughter board **(MTDB)** package contains all components needed for MTDB in conjunction with an Altera FPGA board with HSMC connector.

1.1 Package Contents

The MTDB package includes:

- The Terasic Multimedia Touch Panel daughter board
- MTDB System CD-ROM
- [Optional] Components to assemble the MTDB with a Cyclone III Starter Board into a BRICK format as shown in Figure 1.1. The detailed instructions on how to assemble MTDB with a Cyclone III Starter board into a BRICK format can be found in the *CycloneIII_Starter_Board/BRICK* folder on the **MTDB System CD-ROM**

Figure 1.1. The BRICK form of combining the MTDB to an Altera Cyclone III Starter Board.

1.2 Getting Help

Here are the addresses where you can get help if you encounter problems:

- Altera Corporation
  101 Innovation Drive
  San Jose, California, 95134 USA
  Email: mysupport@altera.com

- Terasic Technologies
  No. 356, Sec. 1, Fusing E. Rd.
  Jhubei City, HsinChu County, Taiwan, 302
  Email: support@terasic.com
  Web: www.terasic.com

Chapter 2
MTDB Hardware Specification

This chapter presents the features and design characteristics of the MTDB hardware.

2.1 Layout and Components

A photograph of the MTDB is shown in Figure 2.1, Figure 2.2, Figure 2.3, and Figure 2.5. These pictures depict the layout of the board and indicate the location of the connectors and key components.

Figure 2.1. The MTDB (Top View)

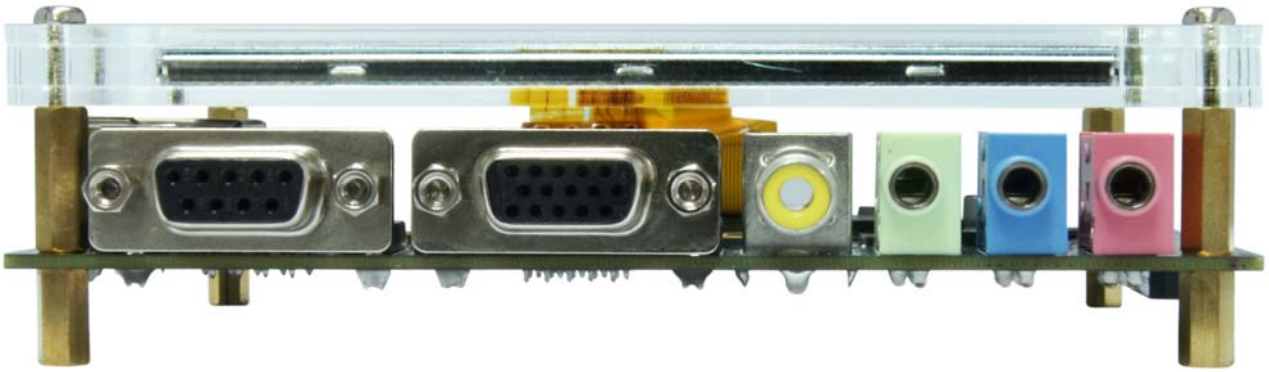

Figure 2.2. The MTDB (Connector view 1)

Figure 2.3. The MTDB (Connector view 2)

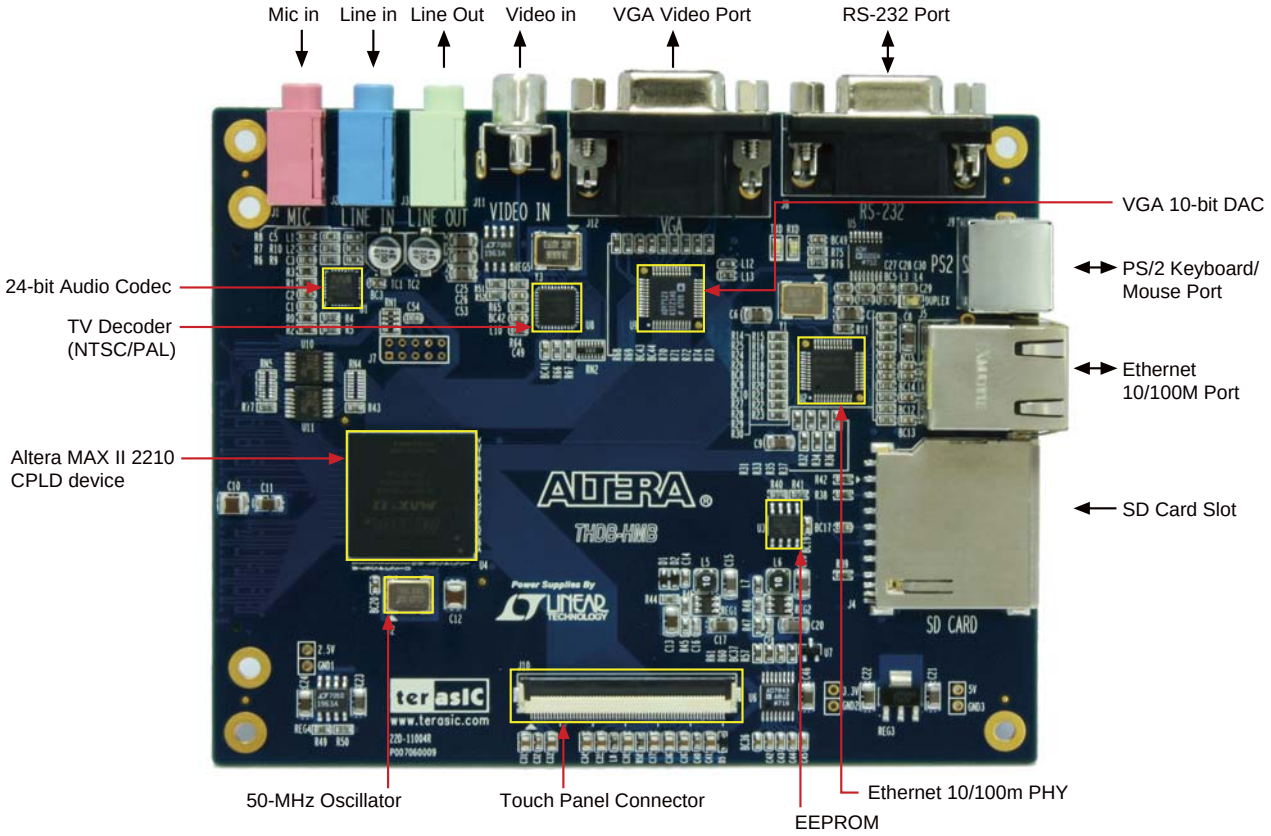

Figure 2.4 The MTDB PCB and Component diagram

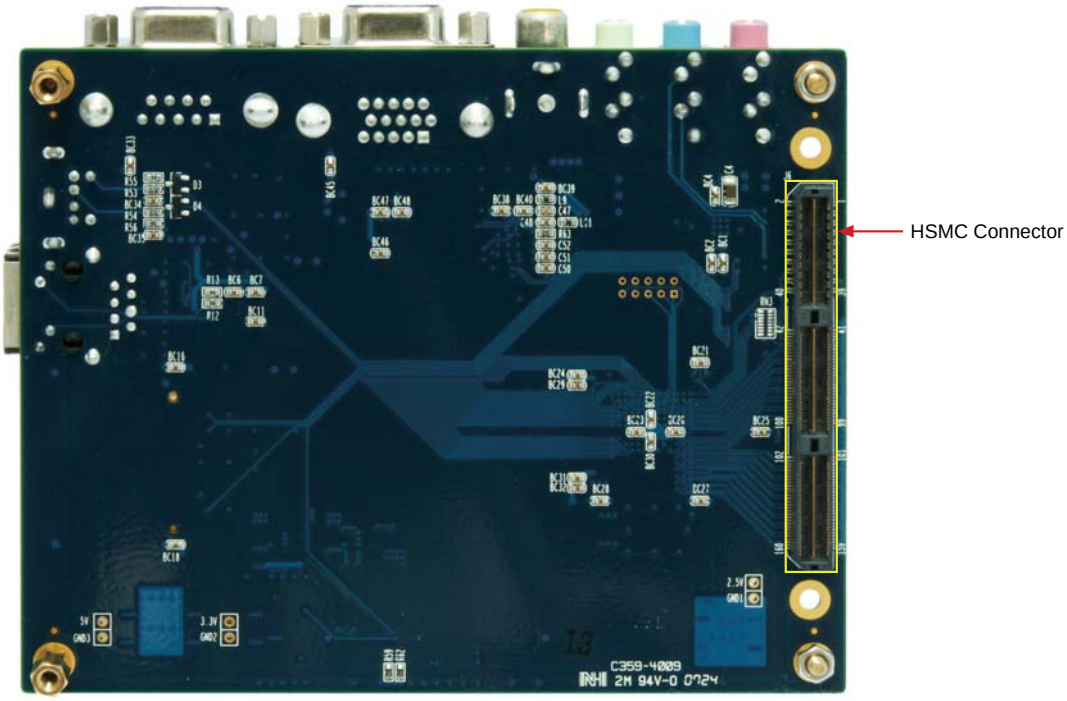

Figure 2.5. The MTDB Back side – HSMC connector view

The MTDB board has many features that allow users to implement a wide range of designed circuits, from simple circuits to various multimedia projects with touch panel applications.

The following hardware is provided on the MTDB board:

- Altera MAX II 2210 CPLD device
- SD Card socket
- 100-MHz oscillator for clock sources
- 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks
- VGA DAC (10-bit high-speed triple DACs) with VGA-out connector
- TV Decoder (NTSC/PAL/SECAM) and TV-in connector
- 10/100 Ethernet Physical Layer Transceiver
- RS-232 transceiver and 9-pin connector
- PS/2 mouse/keyboard connector
- 800x480 Active matrix color TFT LCD Touch Panel module
- I2C Serial EEPROM

To use the MTDB, the user has to be familiar with the Quartus II software.

2.2 Block Diagram of the MTDB

Figure 2.6 gives the block diagram of the MTDB. To provide maximum flexibility for the user, all connections are made through the HSMC connector device. Thus, the user can configure the FPGA on the mother board to implement any system design.

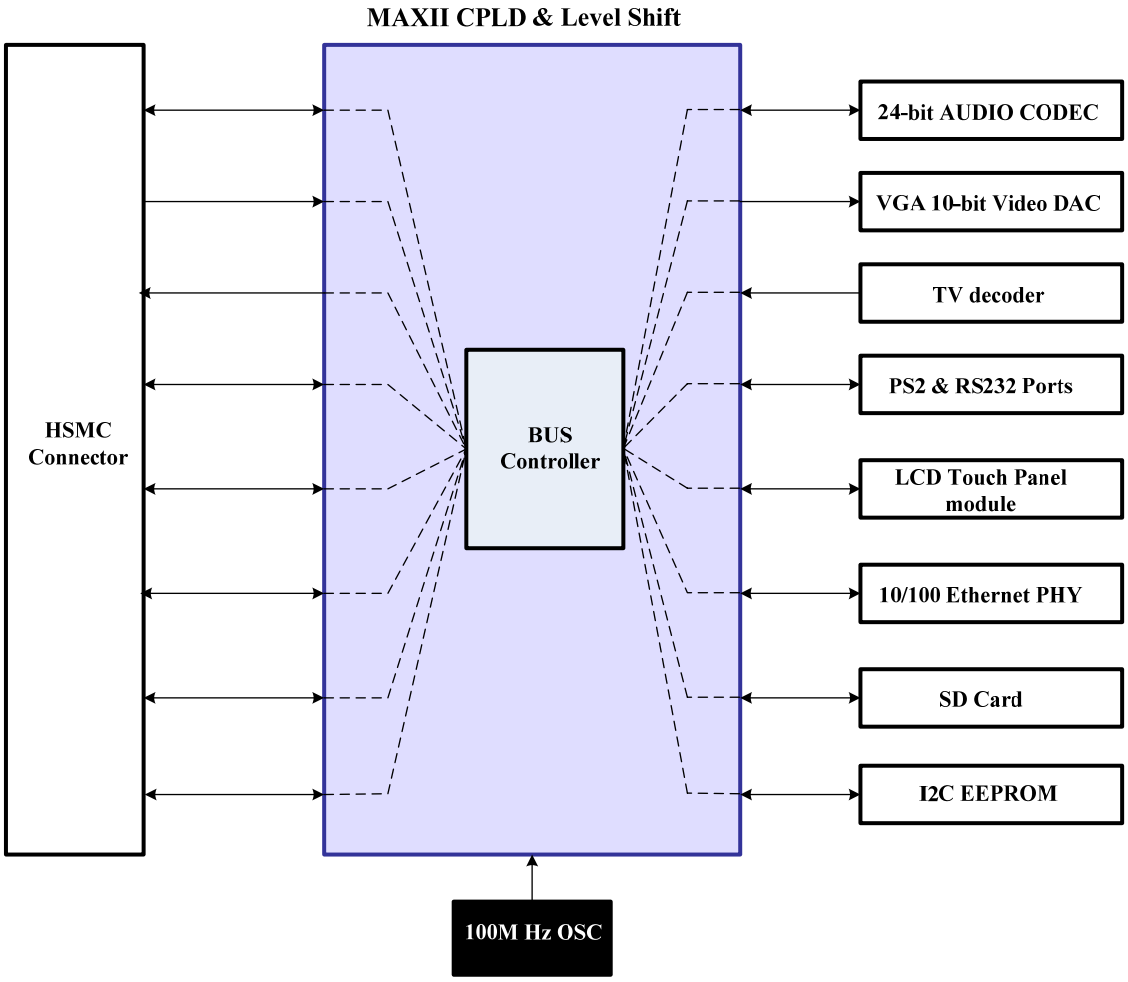

Figure 2.6. Block diagram of the MTDB board.

Following is more detailed information about the blocks in Figure 2.6:

MAX II 2210 CPLD

- 2210 LEs
- 272 user I/O pins
- FineLine BGA 324-pin package

4.3” 800x480 LCD Touch panel Module and Touch Screen Digitizer

- Equipped with Toppoly TD043MTEA1 active matrix color TFT LCD module.
- Uses the Analog Devices AD7843 touch screen digitizer
- Support 24-bit parallel RGB interface.
- 3-wire register control for display and function selection.
- Built-in contrast, brightness and gamma modulation.

SD card socket

- Accessible as memory in both SPI and 1-bit SD modes.

Clock inputs

- 100-MHz oscillator.

Audio CODEC

- Wolfson WM8731 24-bit sigma-delta audio CODEC.
- Line-level input, line-level output, and microphone input jacks.
- Sampling frequency: 8 to 96 KHz.
- Applications for MP3 players and recorders, PDAs, smart phones, voice recorders, etc.

VGA output

- Uses the ADV7123 240-MHz triple 10-bit high-speed video DAC.
- With 15-pin high-density D-sub connector.

NTSC/PAL TV decoder circuit

- Uses the ADV7180 Multi-format SDTV Video Decoder.
- Supports worldwide NTSC/PAL/SECAM color demodulation.
- One 10-bit ADC, 4X over-sampling for CVBS.
- Supports Composite Video (CVBS) RCA jack input.
- Supports digital output formats : 8-bit ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD
- Applications: DVD recorders, LCD TV, Set-top boxes, Digital TV, and Portable video devices

Ethernet Physical Layer Transceiver

- Uses the DP83848C Single Port 10/100 Mb/s Ethernet Physical Layer Transceiver
- Supports both 100Base-T and 10Base-T Ethernet protocols
- Supports Auto-MDIX for 10/100 Mb/s

Serial ports

- One RS-232 port
- One PS/2 port
- DB-9 serial connector for the RS-232 port
- PS/2 connector for connecting a PS2 mouse or keyboard to the MTDB board.

I2C serial EEPROM

- Use one 128 bit EEPROM.
- Supports 2-wire serial interface, I2C compatible.

Chapter 3
MTDB Bus Controller

The MTDB comes with a bus controller that allows a user to access all components on the board through the HSMC connector, without being limited by the number of user IOs of the HSMC connector. This chapter describes its structure in block diagram form, and finally describes its capabilities.

3.1 MTDB Bus Controller Introduction

The two major functions of the MTDB Bus Controller are listed

1. Provide time-division multiplexing functions to the LCD and VGA color data bus.
2. Provide level shifting feature for the 2.5V (Cyclone III FPGA) and 3.3V (the MTDB side) domains.

3.2 Block Design of the MTDB Bus Controller

Figure 3.1 shows the block diagram of MTDB Bus Controller. Both the LCD and VGA TDM blocks are simple 8-bit to 24-bit and 10-bit to 30-bit data de-multiplexing functions respectively, which are final logic driving the LCD panel and VGA DAC. In the LCD TDM block, the 8-bit input data (successive BGR color data) comes in at 3 times the rate of the 24-bit output data bus (8-bit B + 8bit G + 8bit R) we drive to the LCD panel. This function can reduce the pin-count of the HSMC connector. The I2C_Bir_bus block provides bidirectional control for I2C Serial EEPROM data bus.

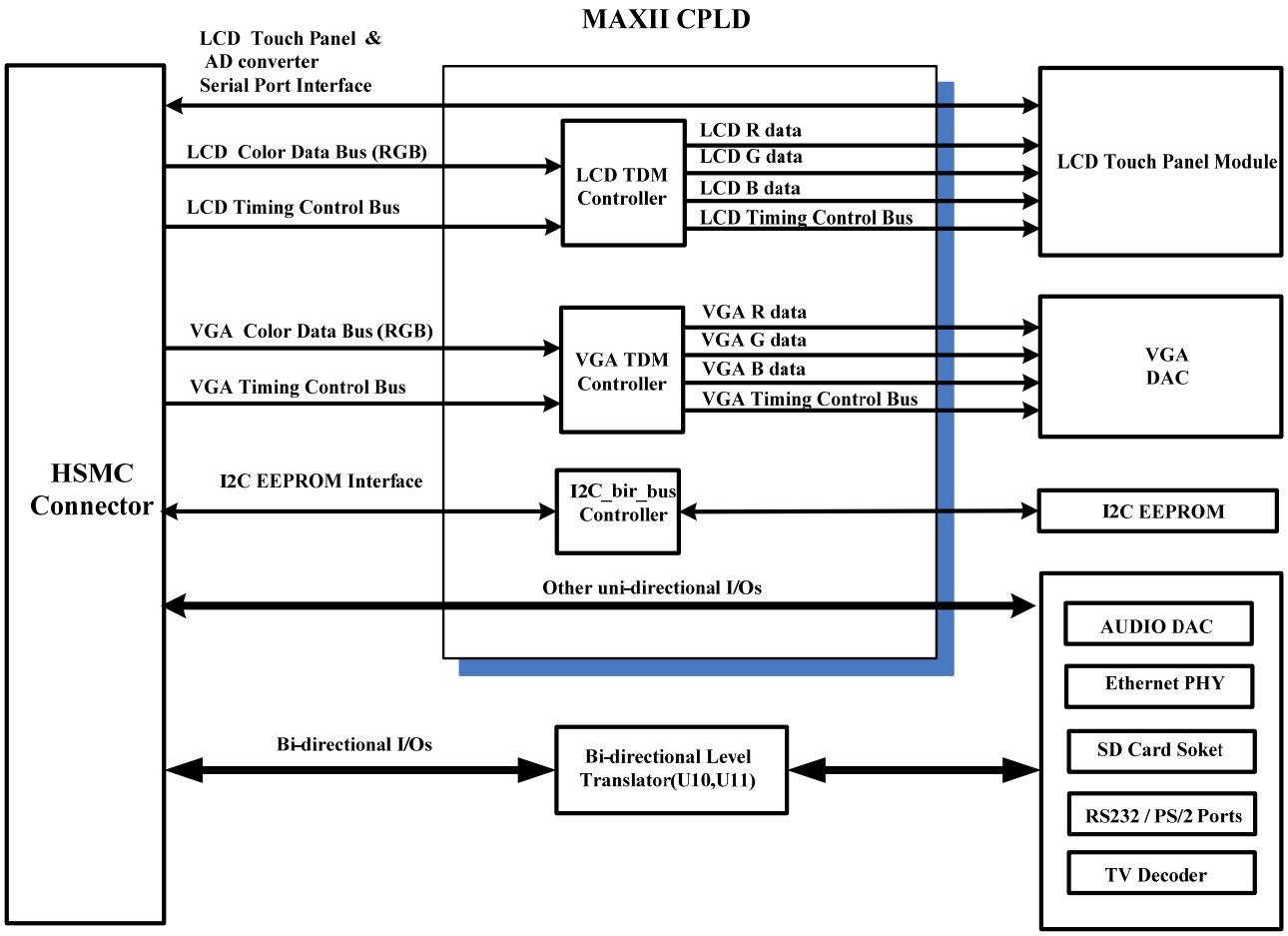

Figure 3.1. The Block Diagram of MTDB Bus Controller

The RTL code of the MTDB Bus Controller can be found in the *MTDB_Bus_Controller/default* folder of the **MTDB System CD-ROM**

3.3 Timing Protocol of the LCD TDM Controller

Figure 3.2 describes the input timing waveform information of the LCD TDM Controller. The 8-bit wide HC_LCD_DATA signal is presumed to contain a stream of color pixel data, with each pixel represented by three successive clock-cycles of the stream. The data is presented as "BGR". The LCD TDM Controller uses the HC_HD pulse to determine the position of the BLUE color sample, and thus the start of each three-clock pixel-period. State transitions on HC_HD (0-->1 or 1-->0) coincide with the presentation of BLUE color on the HC_LCD_DATA input. The GREEN and RED values for that same pixel are presented on the next two clock-cycles. Figure 3.3 shows the timing information from the output side. The LCD TDM block will generate a NCLK clock and 24-bit RGB data to the LCD panel. The NCLK signal runs at 1/3 frequency of the incoming clock HC_NCLK. In addition, the timing protocol of the VGA TDM controller is very similar to the LCD TDM controller. The input color data bus HC_VGA_DATA changes from 8-bit to 10-bit, and the

VGA TDM controller uses the HC_VGA_HS to determine the position of the BLUE color sample.

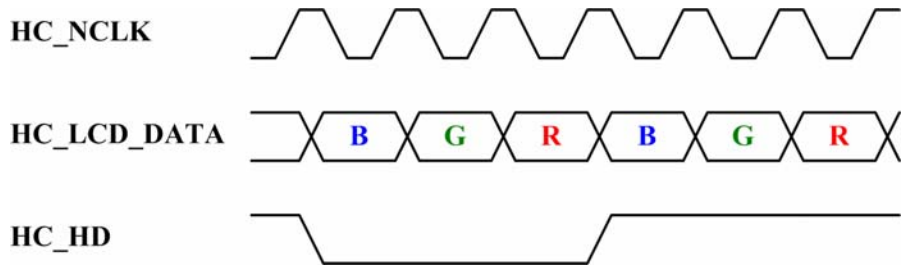

Figure 3.2. The timing diagram shows the input side of the VGA TDM Controller

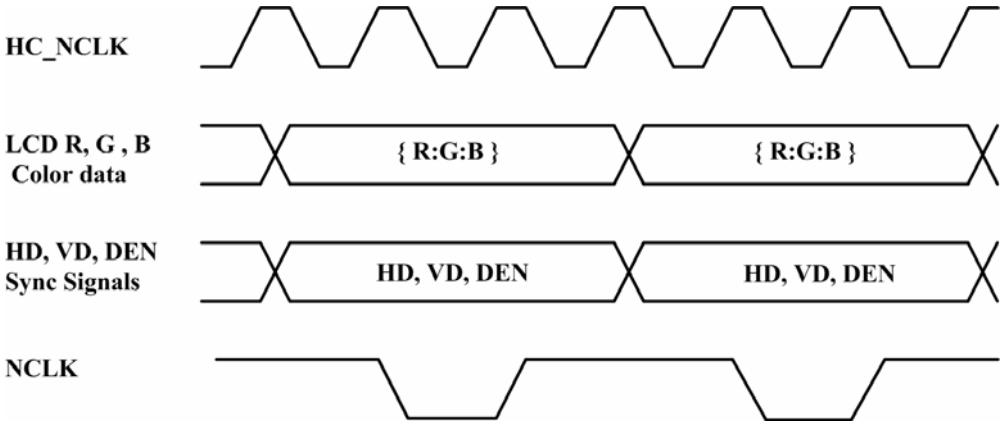

Figure 3.3. The timing diagram shows the output side of the LCD TDM Controller

3.4 Bidirectional level shift interface

The board provides bidirectional level shift feature for the 2.5V input (Cyclone III FPGA) and 3.3V required by many of the interface chips via two Maxim MAX3378 level translators. Table 3.1 lists bidirectional level shift interface reference and manufacturing information. Figure 3.4 shows the block diagram and pinout of the bidirectional level shift interface on the board respectively. Figure 3.5 shows the Level Shift Interface schematic.

HSMC Side Signal Name	HSMC Pin No.	Device Side Signal Name	Device Pin No.	Device Pin No.
HC_I2C_SDAT	33	I2C_SDAT	U1-27;U8-33	Audio CODEC ADC LR Clock
HC_PS2_CLK	43	PS2_CLK	J9-6	PS/2 Clock
HC_PS2_DAT	47	PS2_DAT	J9-1	PS/2 Data
HC_MDIO	49	MDIO	U2-30	Ethernet PHY Management Data I/O
HC_SD_DAT3	53	SD_DAT3	J4-1	SD 1-bit Mode: Card Detect; SPI Mode: Chip Select (Active Low)
HC_SD_CMD	44	SD_CMD	J4-2	SD 1-bit Mode: Command Line; SPI Mode: Data In
HC_SD_DAT	48	SD_DAT	J4-7	SD 1-bit Mode: Data Line; SPI Mode: Data Out
HC_SDA	50	SDA	J10-44	LCD 3-Wire Serial Interface Data

Table 3.1. The timing diagram shows the output side of the LCD TDM Controller

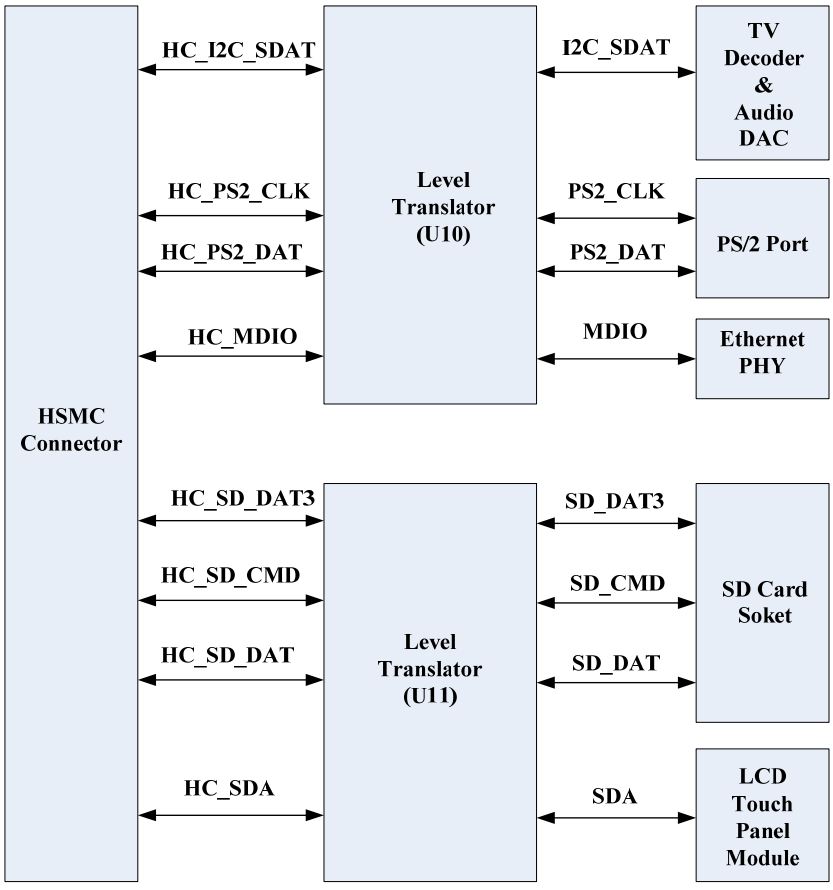

Figure 3.4. The timing diagram shows the output side of the LCD TDM Controller

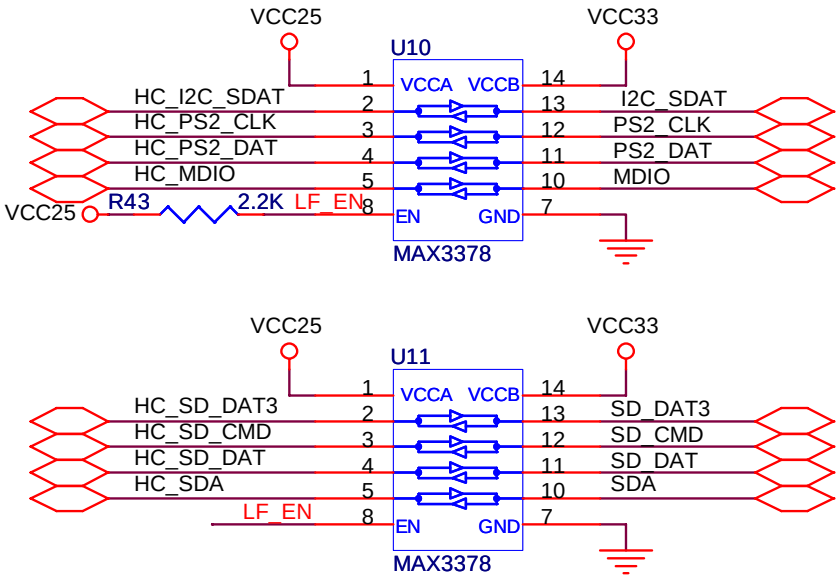

Figure 3.5. Bidirectional level shift interface schematic.

Chapter 4
Using the MTDB

This chapter gives instructions for using MTDB and describes each of its I/O devices. The MTDB is designed for an Altera FPGA board with a HSMC connector. The demonstration projects illustrated here are using MTDB with the latest Cyclone III Starter Board.

4.1 Configuring the Cyclone III Starter Board

The procedure for downloading a circuit from a host computer to the Cyclone III Starter board is described in the Cyclone III Starter Kit User Manual. This tutorial is found in the *CycloneIII_Starter_Kit* folder of the **MTDB System CD-ROM,** and it is also available on the Altera Cyclone III Starter Kit web pages. The user is encouraged to read the tutorial first, and to treat the information below as a short reference.

Figure 4.1 illustrates how to connect your MTDB to a Cyclone III Starter board. To download a configuration bit stream into the Cyclone III FPGA, perform the following steps:

- Ensure that power is applied to the Cyclone III Starter board
- Connect the supplied USB cable to the USB Blaster port on the Cyclone III Starter board
- The FPGA can now be programmed by using the Quartus II Programmer module to select a configuration bit stream file with the *.sof* filename extension

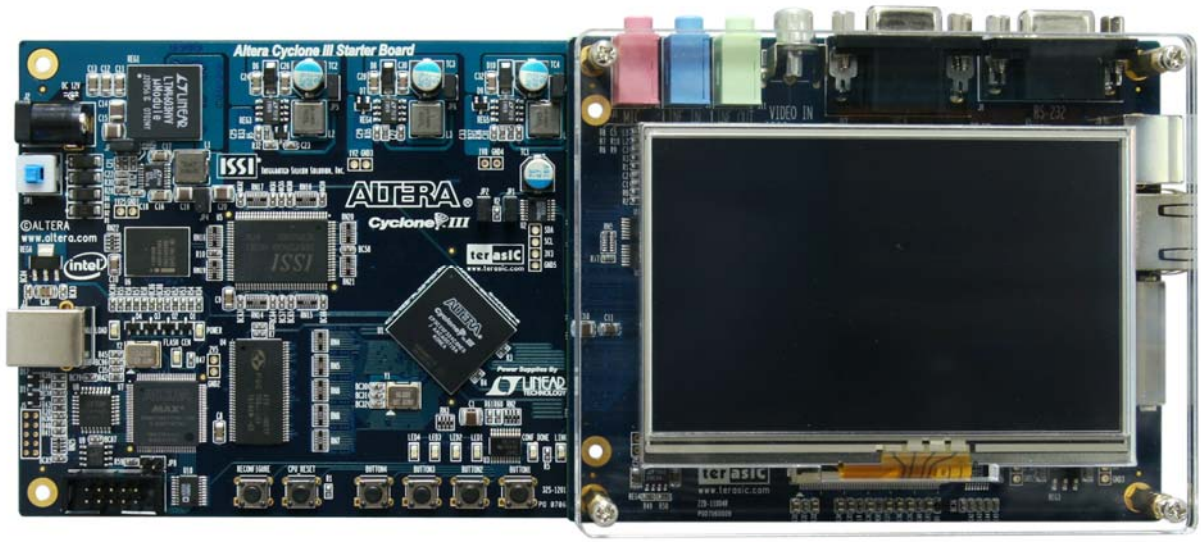

Figure 4.1. Connection of a MTDB Board and a Cyclone III Starter Board.

Users can find the default demonstration project under the *Demonstrations/default* folder in the **MTDB System CD-ROM. Users are also encouraged to examine the top-level RTL code when reading the following sections.**

4.2 Using the 4.3” LCD Touch Panel Module

The MTDB provides a 4.3" Toppoly TD043MTEA1 active matrix color TFT LCD panel. The LCD Touch Panel module has the highest resolution (800x480) to provide users the best display quality for developing applications. The LCD panel supports 24-bit parallel RGB data interface and provides 3-wire serial port interface to control the display function registers.

The MTDB Board is also equipped with an Analog Devices AD7843 touch screen digitizer chip. The AD7843 is a 12-bit analog to digital converter (ADC) for digitizing x and y coordinates of touch points applied to the touch screen. Also, the coordinates of the touch point can be read through the serial port interface on the AD7843. However, because of the limited I/Os of the HSMC connector, the clock signal of the serial port interface for the LCD panel and AD7843 shares the same HSMC connector I/O called HC_ADC_DCLK, **users must not control both LCD panel and AD7843 at the same time.**

To display images on the LCD panel correctly, the first thing users need to do is that the RGB color data and synchronization signals need to follow the timing specification of the LCD Touch panel as shown in Figure 4.2, Figure 4.3, Table 4.1, and Table 4.2. After that, because of the number of user IOs of the HSMC connector are limited. The LCD RGB data and synchronization signals outputted to the MTDB board need to be multiplex to fit the input timing specification of the LCD TDM Controller on the MTDB board as mention in the Section 3.3.

Finally, the associated schematic of the LCD touch panel module is given in Figure 4.4, and the pin assignments are listed in Table 4.3 Detailed information for using the LCD panel and AD7843 are available in their datasheets, which can be found on the *Datasheet* folder of the **MTDB System CD-ROM** or form the manufacturers' web site.

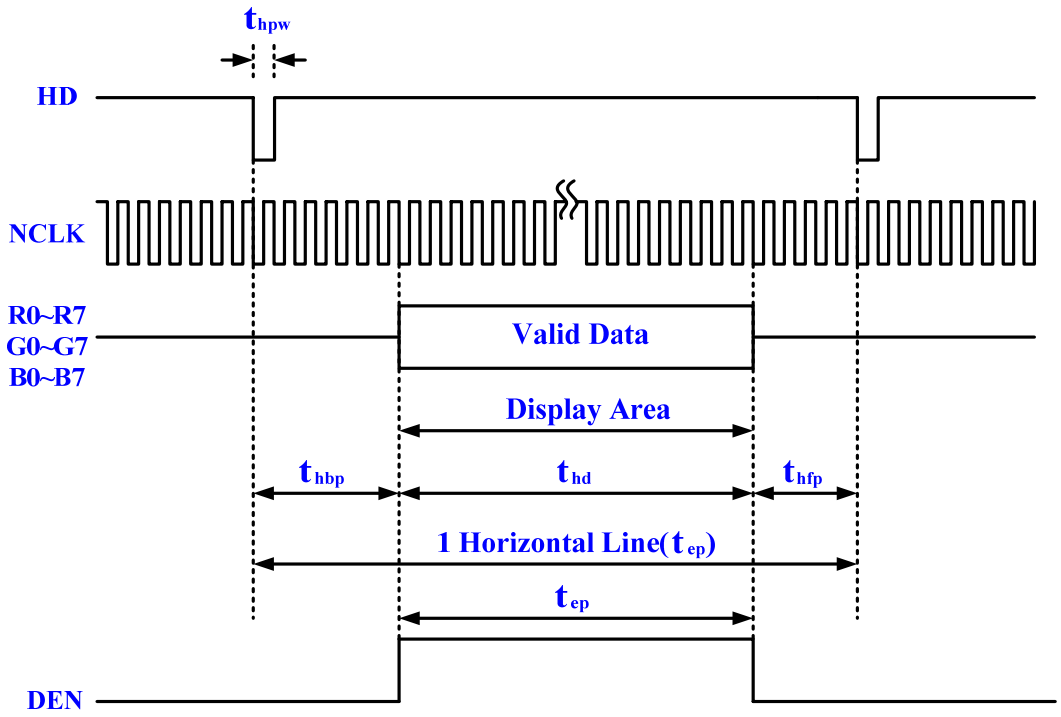

Figure 4.2 LCD horizontal timing specification

Parameter		Symbol	Panel Resolution			Unit
			800xRGBx480	480xRGBx272	400xRGBx240	
NCLK Frequency		FNCLK	33.2	9	8.3	MHz
Horizontal valid data		t_{hd}	800	480	400	NCLK
1 Horizontal Line		t_h	1056	525	528	NCLK
HSYNC Pulse Width	Min.	t_{hpw}	1			NCLK
	Typ.		-			
	Max.		-			
Hsync back porch		t_{hbp}	216	43	108	NCLK
Hsync front porch		t_{hfp}	40	2	20	NCLK
DEN Enable Time		t_{ep}	800	480	400	NCLK

Table 4.1 LCD horizontal timing parameters

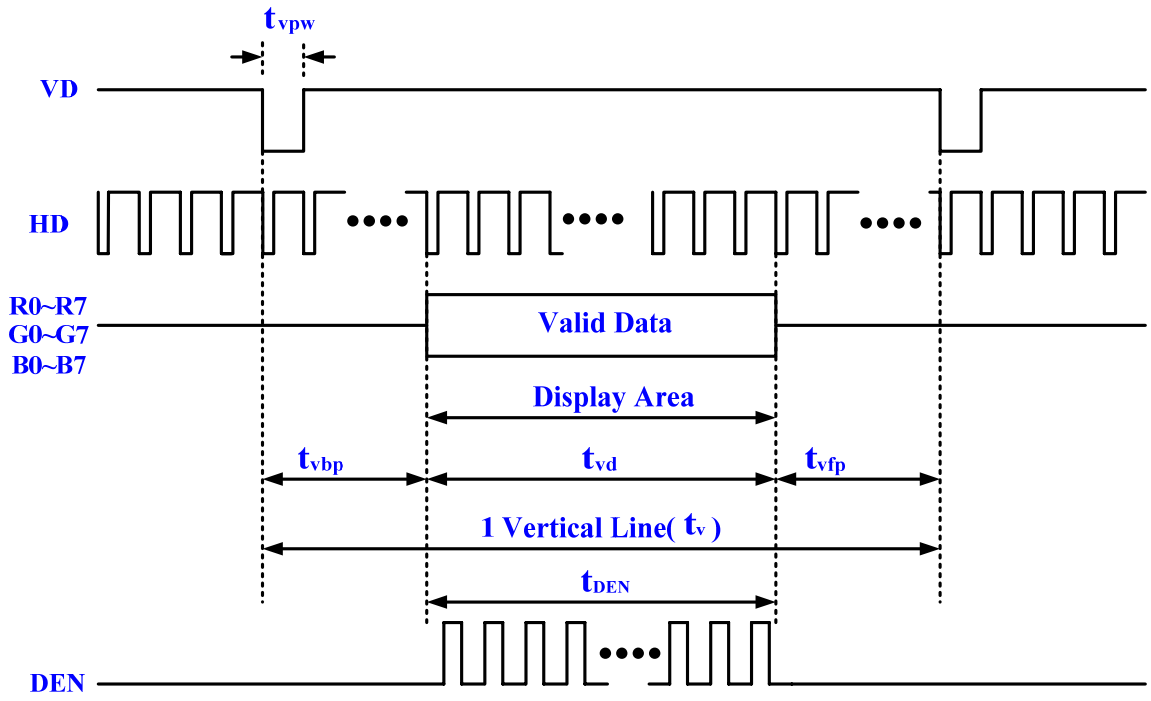

Figure 4.3 LCD vertical timing specification

Parameter		Symbol	Panel Resolution			Unit
			800xRGBx480	480xRGBx272	400xRGBx240	
Vertical valid data		t_{vd}	480	272	240	H
Vertical period		t_{v}	525	286	262	H
VSYNC Pulse Width	Min.	t_{vpw}	1			H
	Typ.		-			
	Max.		-			
Vertical back porch		t_{vbo}	35	12	20	H
Vertical front porch		t_{vfpo}	10	2	2	H
Vertical blanking		t_{vb}	45	14	22	H

Table 4.2 LCD vertical timing parameters

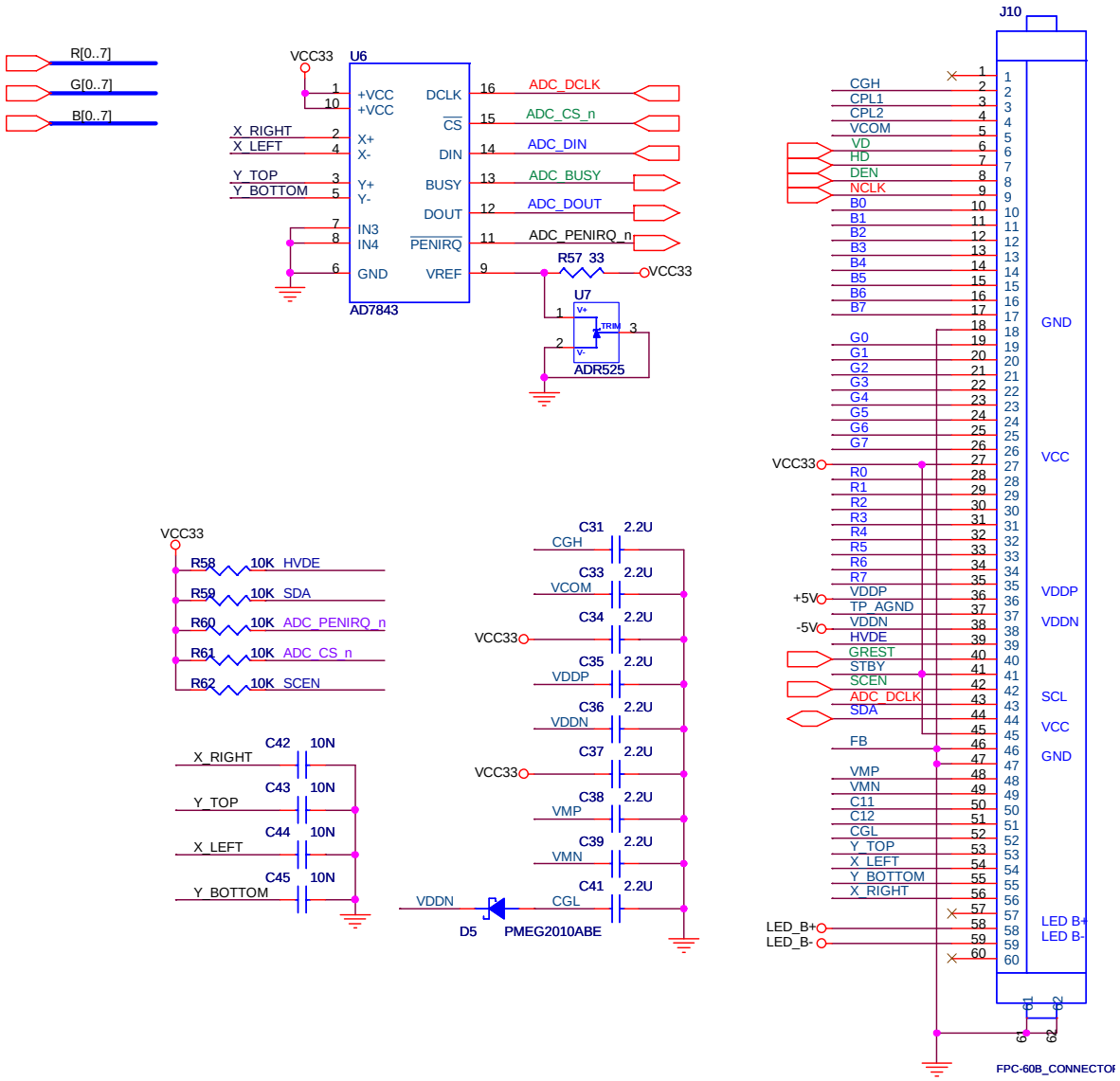

Figure 4.4. Schematic diagram of the LCD Touch Panel Module

HSMC Connector		MAX II		LCD Touch Panel		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_DEN	138	C15	E5	DEN	8	LCD RGB Data Enable
HC_NCLK	95	K13	E4	NCLK	9	LC D Clock
HC_LCD_DATA[0]	145	D17	H1	R[0]	28	LCD red data bus bit 0
			E3	G[0]	19	LCD green data bus bit 0
			D4	B[0]	10	LCD blue data bus bit 0
HC_LCD_DATA[1]	149	C17	H2	R[1]	29	LCD red data bus bit 1
			F3	G[1]	20	LCD green data bus bit 1
			C3	B[1]	11	LCD blue data bus bit 1

HSMC Connector		MAX II		LCD Touch Panel		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_LCD_DATA[2]	151	C16	J2	R[2]	30	LCD red data bus bit 2
			F1	G[2]	21	LCD green data bus bit 2
			C2	B[2]	12	LCD blue data bus bit 2
HC_LCD_DATA[3]	126	D13	J1	R[3]	31	LCD red data bus bit 3
			F2	G[3]	22	LCD green data bus bit 3
			D3	B[3]	13	LCD blue data bus bit 3
HC_LCD_DATA[4]	128	D15	J3	R[4]	32	LCD red data bus bit 4
			G2	G[4]	23	LCD green data bus bit 4
			D1	B[4]	14	LCD blue data bus bit 4
HC_LCD_DATA[5]	146	B15	K3	R[5]	33	LCD red data bus bit 5
			G1	G[5]	24	LCD green data bus bit 5
			D2	B[5]	15	LCD blue data bus bit 5
HC_LCD_DATA[6]	150	B14	K1	R[6]	34	LCD red data bus bit 6
			G3	G[6]	25	LCD green data bus bit 6
			E2	B[6]	16	LCD blue data bus bit 6
HC_LCD_DATA[7]	152	A15	K2	R[7]	35	LCD red data bus bit 7
			H3	G[7]	26	LCD green data bus bit 7
			E1	B[7]	17	LCD blue data bus bit 7
HC_GREST	140	C13	L2	GREST	40	LCD Global Reset, Low Active
HC_SCEN	144	B13	L1	SCEN	42	LCD 3-Wire Serial Interface Enable
HC_SDA	50	U11-5 (*1)	U11-10 (*1)	SDA	J10.44	LCD 3-Wire SerialInterface Data
HC_ADC_DCLK	157	B18	L3	ADC_DCLK	U6.16	AD7843/LCD 3-Wire Serial Interface Clock
HC_ADC_DIN	155	B16	N2	ADC_DIN	U6.14	AD7843 Serial Interface Data In
HC_ADC_CS_n	143	D18	N1	ADC_CS_n	U6.15	AD7843 Serial Interface Chip Select Input
HC_ADC_DOUT	122	E13	M1	ADC_DOUT	U6.12	AD7843 Serial Interface Data Out
HC_ADC_PENIRQ_n	156	A14	M3	ADC_PENIRQ_n	U6.11	AD7843 pen Interrupt
HC_ADC_BUSY	120	E15	M2	ADC_BUSY	U6.13	AD7843 Serial Interface Busy
Notes:(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U11.						

Table 4.3. Pin assignments for the LCD Touch Panel Module

4.3 Using VGA

The MTDB includes a 16-pin D-SUB connector for VGA output. The VGA synchronization signals are provided directly from the Cyclone III FPGA, and the Analog Devices ADV7123 triple 10-bit high-speed video DAC is used to produce the analog data signals (red, green, and blue). The associated schematic is given in Figure 4.5.

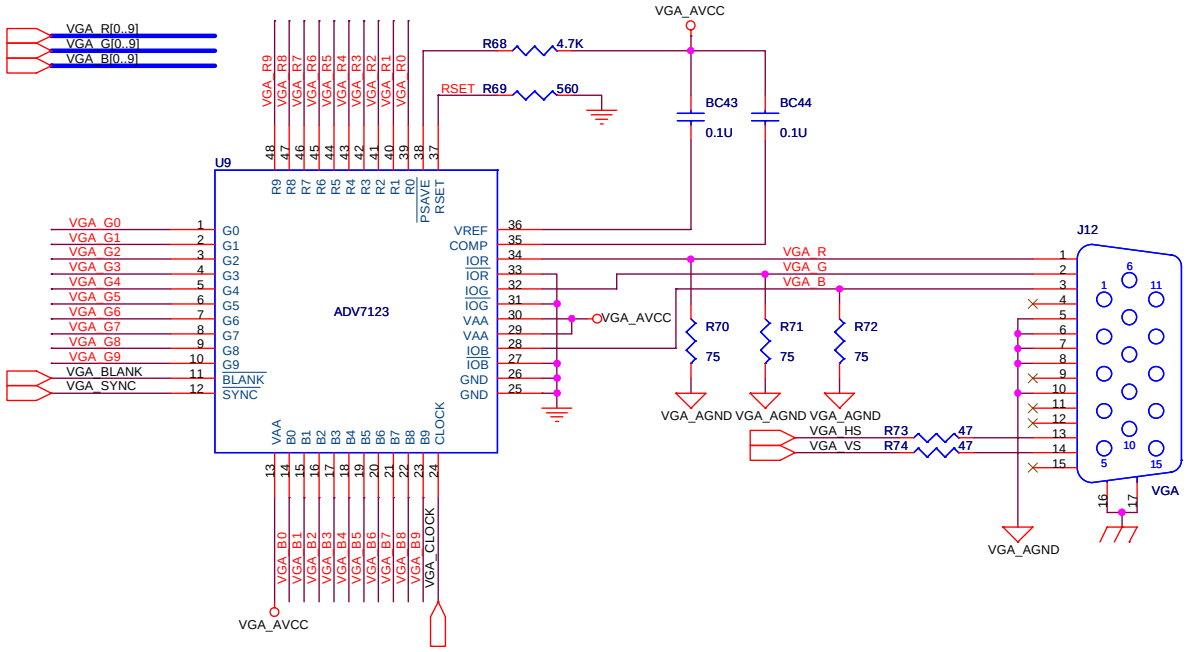

Figure 4.5. VGA circuit schematic.

The timing specification for VGA synchronization and RGB (red, green, blue) data can be found on various educational web sites (for example, search for “VGA signal timing”). Figure 4.6 illustrates the basic timing requirements for each row (horizontal) that is displayed on a VGA monitor. An active-low pulse of specific duration (time *a* in the figure) is applied to the horizontal synchronization (*hsync*) input of the monitor, which signifies the end of one row of data and the start of the next. The data (RGB) inputs on the monitor must be off (driven to 0 V) for a time period called the *back porch* (*b*) after the *hsync* pulse occurs, which is followed by the display interval (*c*). During the data display interval the RGB data drives each pixel in turn across the row being displayed. Finally, there is a time period called the *front porch* (*d*) where the RGB signals must again be off before the next *hsync* pulse coming up. The timing of the vertical synchronization (*vsync*) is same as shown in Figure 4.6, except that a *vsync* pulse signifies the end of one frame and the start of the next. The data refers to a set of rows in the frame (horizontal timing). Table 4.4 and Table 4.5 show for different resolutions, the durations of time periods *a*, *b*, *c*, and *d* for both horizontal and vertical timing. Note that because of the number of user IOs of the HSMC connector are limited, users need to multiplex the VGA synchronization signals and RGB data to fit the input timing specification of the VGA TDM block as mention in Section 3.3.

Detailed information for using the ADV7123 video DAC is available in its datasheet, which can be found on the manufacturer's web site, and from the *Datasheet* folder of the **MTDB System CD-ROM**. The pin assignments are listed in Table 4.6. An example of code that drives a VGA display is described in Sections 5.2 and 5.3.

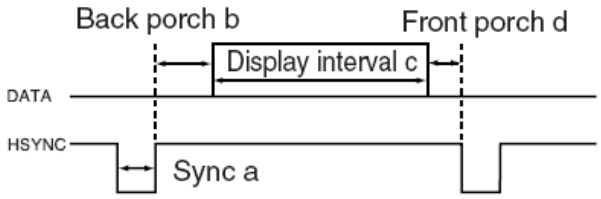

Figure 4.6. VGA horizontal timing specification.

VGA mode		Horizontal Timing Spec				
Configuration	Resolution(HxV)	a(us)	b(us)	c(us)	d(us)	Pixel clock(Mhz)
VGA(60Hz)	640x480	3.8	1.9	25.4	0.6	25 (640/c)
VGA(85Hz)	640x480	1.6	2.2	17.8	1.6	36 (640/c)
SVGA(60Hz)	800x600	3.2	2.2	20	1	40 (800/c)
SVGA(75Hz)	800x600	1.6	3.2	16.2	0.3	49 (800/c)
SVGA(85Hz)	800x600	1.1	2.7	14.2	0.6	56 (800/c)
XGA(60Hz)	1024x768	2.1	2.5	15.8	0.4	65 (1024/c)
XGA(70Hz)	1024x768	1.8	1.9	13.7	0.3	75 (1024/c)
XGA(85Hz)	1024x768	1.0	2.2	10.8	0.5	95 (1024/c)
1280x1024(60Hz)	1280x1024	1.0	2.3	11.9	0.4	108 (1280/c)

Table 4.4. VGA horizontal timing specification.

VGA mode		Vertical Timing Spec			
Configuration	Resolution (HxV)	a(lines)	b(lines)	c(lines)	d(lines)
VGA(60Hz)	640x480	2	33	480	10
VGA(85Hz)	640x480	3	25	480	1
SVGA(60Hz)	800x600	4	23	600	1
SVGA(75Hz)	800x600	3	21	600	1
SVGA(85Hz)	800x600	3	27	600	1
XGA(60Hz)	1024x768	6	29	768	3
XGA(70Hz)	1024x768	6	29	768	3
XGA(85Hz)	1024x768	3	36	768	1
1280x1024(60Hz)	1280x1024	3	38	1024	1

Table 4.5. VGA vertical timing specification.

HSMC Connector		MAX II		LCVGA/DAC Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_VGA_DATA[0]	65	N16	U7	VGA_R0	39	VGA red data bus bit 0
			V4	VGA_G0	1	VGA green data bus bit 0
			R7	VGA_B0	14	VGA blue data bus bit 0
HC_VGA_DATA[1]	67	M16	V7	VGA_R1	40	VGA red data bus bit 1
			U4	VGA_G1	2	VGA green data bus bit 1
			P6	VGA_B1	15	VGA blue data bus bit 1
HC_VGA_DATA[2]	71	M18	T7	VGA_R2	41	VGA red data bus bit 2
			U3	VGA_G2	3	VGA green data bus bit 2
			R6	VGA_B2	16	VGA blue data bus bit 2
HC_VGA_DATA[3]	73	M17	T6	VGA_R3	42	VGA red data bus bit 3
			V2	VGA_G3	4	VGA green data bus bit 3
			R5	VGA_B3	17	VGA blue data bus bit 3
HC_VGA_DATA[4]	77	L17	V6	VGA_R4	43	VGA red data bus bit 4
			P8	VGA_G4	5	VGA green data bus bit 4
			N4	VGA_B4	18	VGA blue data bus bit 4
HC_VGA_DATA[5]	79	L18	U6	VGA_R5	44	VGA red data bus bit 5
			R9	VGA_G5	6	VGA green data bus bit 5
			N5	VGA_B5	19	VGA blue data bus bit 5
HC_VGA_DATA[6]	83	L16	U5	VGA_R6	45	VGA red data bus bit 6
			P9	VGA_G6	7	VGA green data bus bit 6
			M5	VGA_B6	20	VGA blue data bus bit 6
HC_VGA_DATA[7]	85	K16	V5	VGA_R7	46	VGA red data bus bit 7
			P10	VGA_G7	8	VGA green data bus bit 7
			M4	VGA_B7	21	VGA blue data bus bit 7
HC_VGA_DATA[8]	152	K18	T5	VGA_R8	47	VGA red data bus bit 8
			R10	VGA_G8	9	VGA green data bus bit 8
			M6	VGA_B8	22	VGA blue data bus bit 8
HC_VGA_DATA[9]	91	J18	T4	VGA_R9	48	VGA red data bus bit 9
			P11	VGA_G9	10	VGA green data bus bit 9
			L6	VGA_B9	23	VGA blue data bus bit 9
HC_VGA_BLANK	59	N17	R8	VGA_BLANK	11	VGA BLANK
HC_VGA_SYNC	61	N18	P7	VGA_SYNC	12	VGA SYNC
HC_VGA_CLOCK	97	J13	L4	VGA_CLOCK	24	VGA TDM Clock

Table 4.6. ADV7123 pin assignments.

4.4 Using the 24-bit Audio CODEC

The MTDB provides high-quality 24-bit audio via the Wolfson WM8731 audio CODEC (ENCoder/DECoder). This chip supports microphone-in, line-in, and line-out ports, with a sample rate adjustable from 8 kHz to 96 kHz. The WM8731 is controlled by a serial I2C bus interface, which is connected to pins on the HSMC connector. A schematic diagram of the audio circuitry is shown in Figure 4.7, and the pin assignments are listed in Table 4.4. Detailed information for using the WM8731 codec is available in its datasheet, which can be found on the *Datasheet* folder of the **MTDB System CD-ROM** or from the manufacturers' web site.

Note that the direction of the signals HC_AUD_BLCK, HC_AUD_DACLRCK, and HC_AUD_ADCLRCK in the MAXII CPLD are from HSMC connector to the WM8731 codec. Therefore, the WM8731 codec only works in Slave mode. If users need the WM8731 codec works in the Master mode, users can modify the direction of the HC_AUD_BCLK in the MAXII CPLD RTL code which can be found in the *MTDB_Bus_Controller/default* folder on the **MTDB System CD-ROM.**

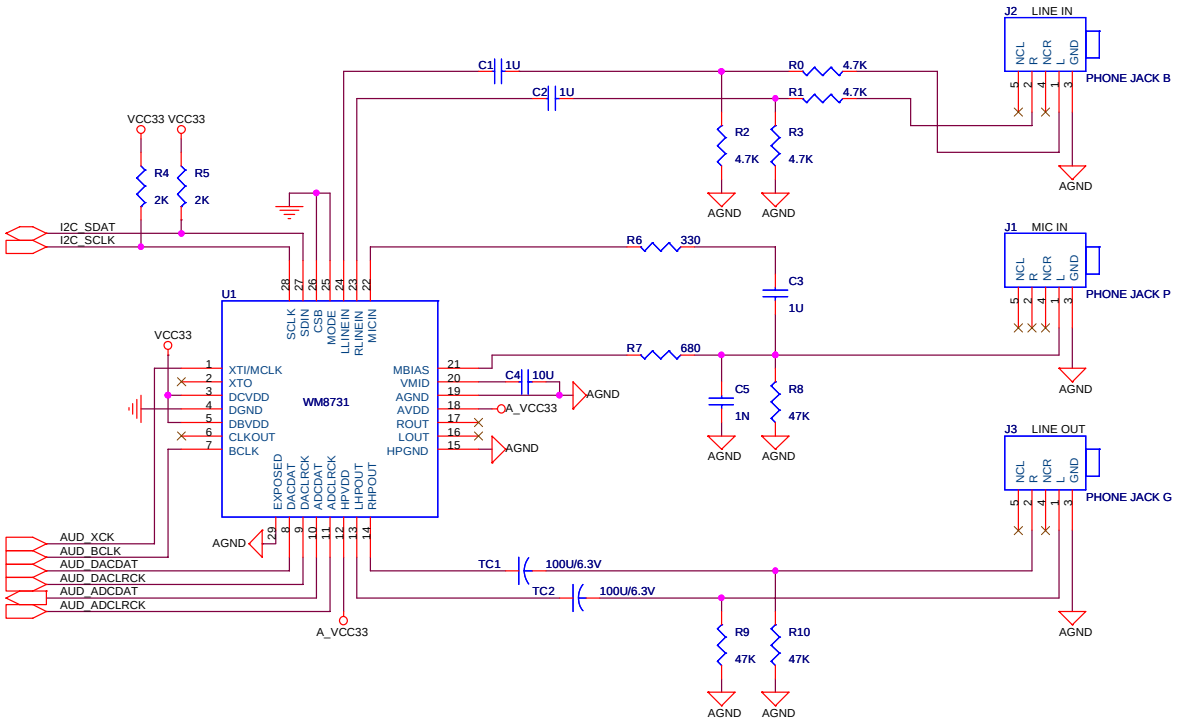

Figure 4.7. Audio CODEC schematic.

HSMC Connector		MAX II		Audio Codec		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_AUD_BCLK	113	G17	U13	AUD_BCLK	7	Audio CODEC Bit-Stream Clock
HC_AUD_XCK	39	T16	U14	AUD_XCK	1	Audio CODEC Chip Clock
HC_AUD_DACDAT	109	H17	V13	AUD_DACDAT	8	Audio CODEC DAC Data
HC_AUD_DACLRCK	107	H18	T13	AUD_DACLRCK	9	Audio CODEC DAC LR Clock
HC_AUD_ADCDAT	40	R15	T12	AUD_ADCDAT	10	Audio CODEC ADC Data
HC_AUD_ADCLRCK	103	H16	V12	AUD_ADCLRCK	11	Audio CODEC ADC LR Clock
HC_I2C_SDAT	33	U10-2 (*1)	U10-13 (*1)	I2C_SDAT	27	I2C Data
HC_I2C_SCLK	34	P15	U11	I2C_SCLK	28	I2C Clock
Notes: (*1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.						

Table 4.7. Audio CODEC pin assignments.

4.5 RS-232 Serial Port

The MTDB board uses the ADM3202 transceiver chip and a 9-pin D-SUB connector for RS-232 communications. For detailed information on how to use the transceiver, please refer to the datasheet, which is available on the *Datasheet* folder of the **MTDB System CD-ROM** or from the manufacturers' web site. Figure 4.8 shows the related schematics, and Table 4.8 lists the HSMC pin assignments.

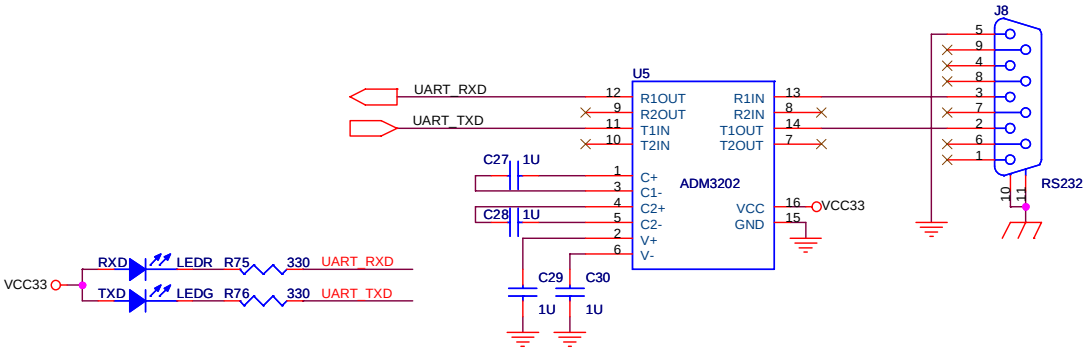

Figure 4.8. ADM3202 (RS-232) schematic.

HSMC Connector		MAX II		RS232 Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_UART_RXD	115	G18	K4	UART_RXD	U5-12 (*1)	UART Receiver
HC_UART_TXD	119	G16	J4	UART_TXD	U5-11 (*2)	UART Transmitter
Notes (*1) U5.12 connects to pin 3 on the RS-232 connector (J6) via U5.13. (*2) U5.11 connects to pin 2 on the RS-232 connector (J6) via U5.14.						

Table 4.8. RS-232 pin assignments.

4.6 PS/2 Serial Port

The MTDB includes a standard PS/2 interface and a connector for a PS/2 keyboard or mouse. Figure 4.9 shows the schematic of the PS/2 circuit. Instructions for using a PS/2 mouse or keyboard can be found by performing an appropriate search on various educational web sites. The pin assignments for the associated interface are shown in Table 4.9.

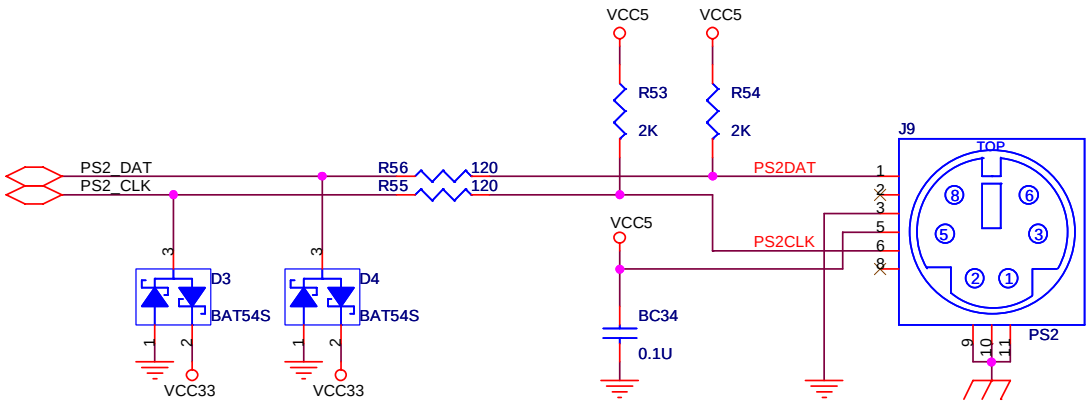

Figure 4.9. PS/2 schematic.

HSMC Connector		MAX II		PS/2 Interface		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_PS2_CLK	43	U10-3 (*1)	U10-12 (*1)	PS2_CLK	1	PS/2 Clock
HC_PS2_DAT	47	U10-4 (*1)	U10-11 (*1)	PS2_DAT	6	PS/2 Data
Notes: (*1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.						

Table 4.9. PS/2 pin assignments.

4.7 Ethernet Physical Layer Transceiver

The MTDB board provides Ethernet support via the National Semiconductor DP83848C Ethernet Physical Layer Transceiver chip. The DP83848C is a one port Fast Ethernet PHY Transceiver supporting IEEE 802.3 physical layer applications at 10Mbps and 100Mbps. The DP83848C provides Media Independent Interface (MII) to connect DP83848C to a MAC in 10/100Mbps systems. Figure 4.10 shows the schematic for the Ethernet Physical Layer Transceiver interface, and the associated pin assignments are listed in Table 4.10. For detailed information on how to use the DP83848C, please refer to its datasheet and application note, which are available on the *Datasheet* folder of the **MTDB System CD-ROM** or from the manufacturers' web site.

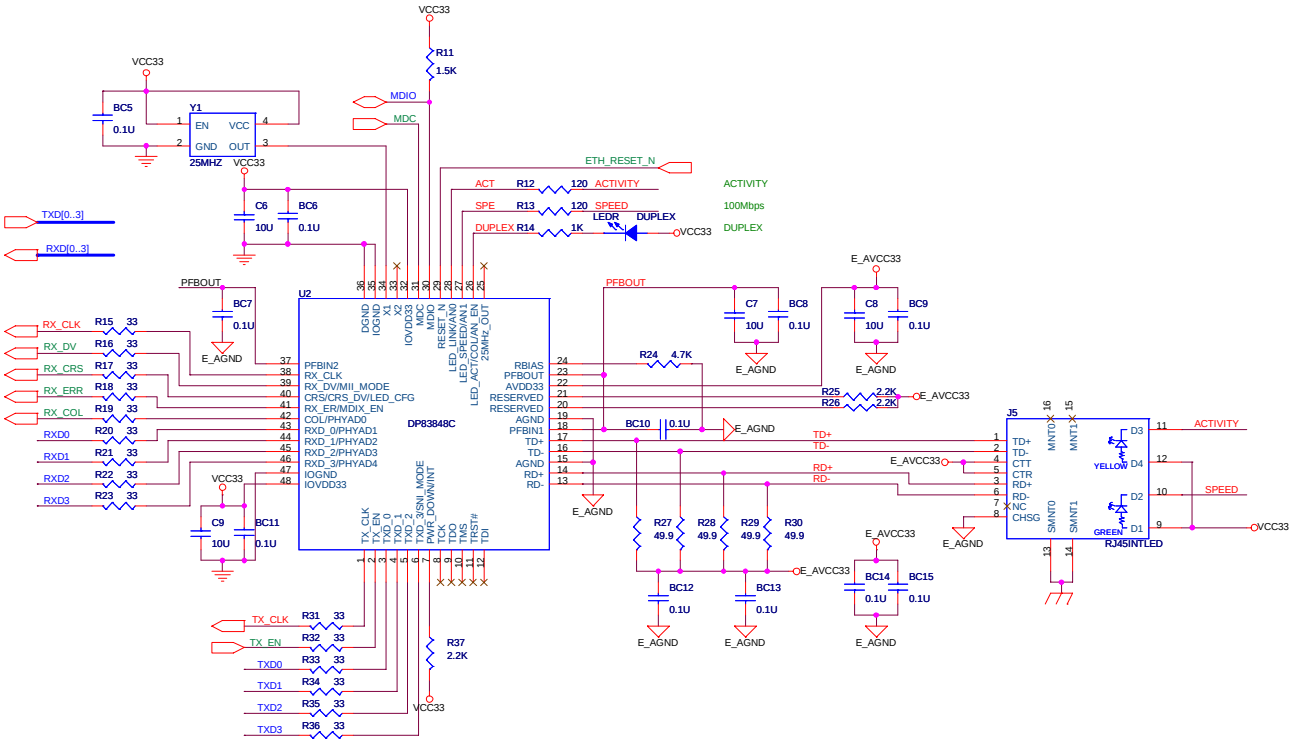

Figure 4.10. Fast Ethernet schematic.

HSMC Connector		MAX II		Ethernet PHY		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_TX_CLK	158	A13	T2	TX_CLK	1	MII Transmit Clock
HC_TX_EN	125	F18	R3	TX_EN	2	MII Transmit Enable
HC_TXD[0]	127	F17	P4	TXD0	3	MII Transmit Data bit 0
HC_TXD[1]	131	E17	R1	TXD1	4	MII Transmit Data bit 1
HC_TXD[2]	133	E18	R2	TXD2	5	MII Transmit Data bit 2
HC_TXD[3]	137	E16	P2	TXD3	6	MII Transmit Data bit 3
HC_ETH_RESET_N	121	F16	T3	Eth_RESET_N	29	DP83848C Reset
HC_MDIO	49	U10-5(*1)	U10-10(*1)	MDIO	30	Management Data I/O
HC_MDC	139	D16	U1	MDC	31	Management Data Clock
HC_RX_CLK	96	H14	J5	RX_CLK	38	MII Receive Clock
HC_RX_DV	116	E14	H5	RX_DV	39	MII Receive Data valid
HC_RX_CRS	92	H15	H4	RX_CRS	40	MII Carrier Sense
HC_RX_ERR	90	G13	H6	RX_ERR	41	MII Receive Error
HC_RX_COL	114	F14	G6	RX_COL	42	MII Collision Detect
HC_RXD[0]	102	G15	G4	RXD0	43	MII Receive Data bit 0
HC_RXD[1]	104	G12	G5	RXD1	44	MII Receive Data bit 1
HC_RXD[2]	108	F13	G7	RXD2	45	MII Receive Data bit 2
HC_RXD[3]	110	F15	F4	RXD3	46	MII Receive Data bit 3
Notes: (*1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.						

Table 4.10. Fast Ethernet pin assignments.

4.8 Digital TV Decoder

The MTDB is equipped with an Analog Devices ADV7180 TV decoder chip. The ADV7180 is an integrated video decoder that automatically detects and converts a standard analog baseband television signal (NTSC, PAL, and SECAM) into 4:2:2 component video data, which is compatible with 8-bit CCIR601/CCIR656. The ADV7180 is compatible with a broad range of video devices, including DVD players, tape-based sources, broadcast sources, and security/surveillance cameras.

The registers in the TV decoder can be programmed by a serial I2C bus, which is connected to the HSMC connector as indicated in Figure 4.11. The pin assignments are listed in Table 4.11. Detailed information on the ADV7180 is available on the *Datasheet* folder of the **MTDB System CD-ROM**

or from the manufacturers' web site.

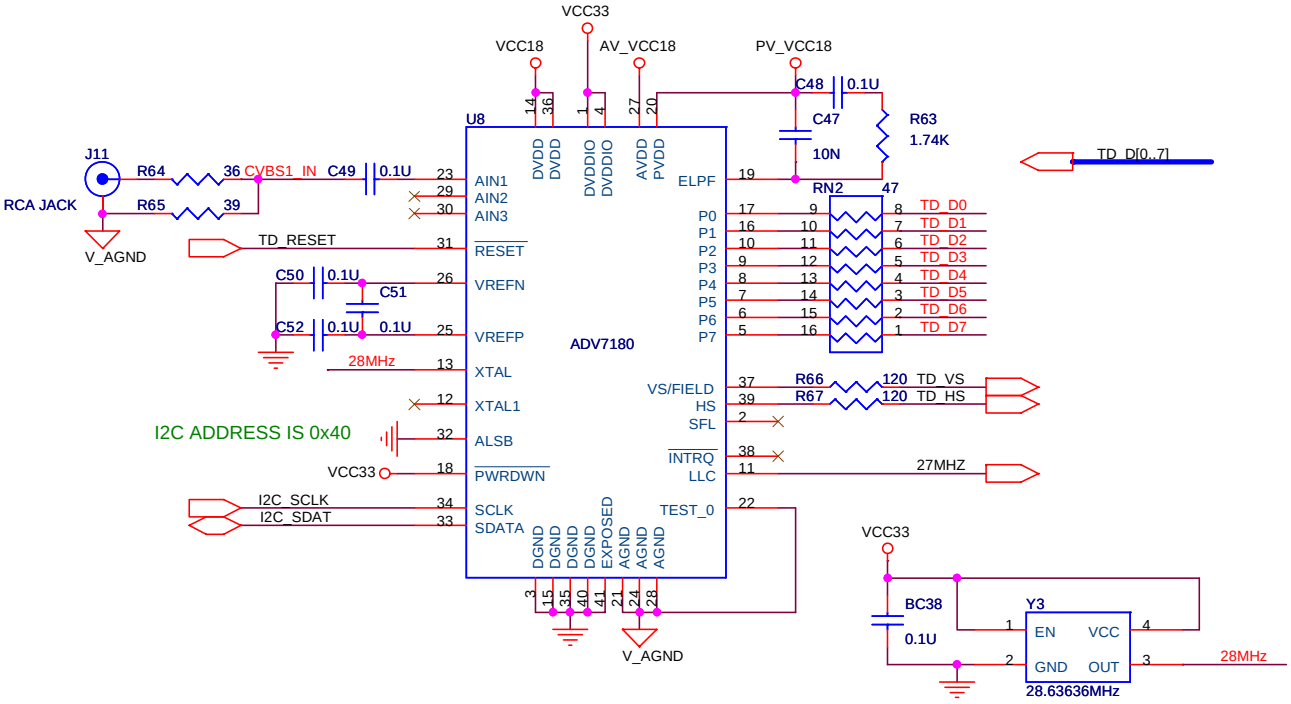

Figure 4.11. Digital TV Decoder schematic.

HSMC Connector		MAX II		Video Decoder		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_TD_D[7]	78	K14	T10	TD_D7	5	Video Decoder Data[7]
HC_TD_D[6]	74	K15	V10	TD_D6	6	Video Decoder Data[6]
HC_TD_D[5]	72	L13	U10	TD_D5	7	Video Decoder Data[5]
HC_TD_D[4]	68	M12	U9	TD_D4	8	Video Decoder Data[4]
HC_TD_D[3]	66	L15	V9	TD_D3	9	Video Decoder Data[3]
HC_TD_D[2]	62	L14	T9	TD_D2	10	Video Decoder Data[2]
HC_TD_D[1]	60	M14	T8	TD_D1	16	Video Decoder Data[1]
HC_TD_D[0]	56	M15	V8	TD_D0	17	Video Decoder Data[0]
HC_TD_27MHZ	98	G14	U8	TD_27MHZ	11	I2C Clock
HC_TD_RESET	80	J14	U12	TD_RESET	31	Video Decoder Reset
HC_I2C_SDAT	33	U10-2 (*1)	U10-13 (*1)	I2C_DATA	33	I2C Data
HC_I2C_SCLK	34	P15	U11	I2C_SCLK	34	Video Decoder Clock Input
HC_TD_VS	84	J15	V11	TD_VS	37	Video Decoder V_SYNC
HC_TD_HS	86	H13	T11	TD_HS	39	Video Decoder H_SYNC
***Notes :**(1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U10.						

Table 4.11. TV Decoder pin assignments.

4.9 I2C Serial EEPROM

The MTDB uses a Microchip 128-bit I2C serial EEPROM to store the MAC address and the boundary parameters of the touch panel for the Ethernet operation and touch panel respectively. The EEPROM is programmed by I2C serial Interface, which is connected through the CPLD to the HSMC connector. Figure 4.12 shows the schematic of the I2C Serial EEPROM, and the associated pin assignments are listed in Table 4.12. Detailed information for using the I2C EEPROM is available in its datasheet, which can be found on the *Datasheet* folder of the **MTDB System CD-ROM** or from the manufacturers' web site.

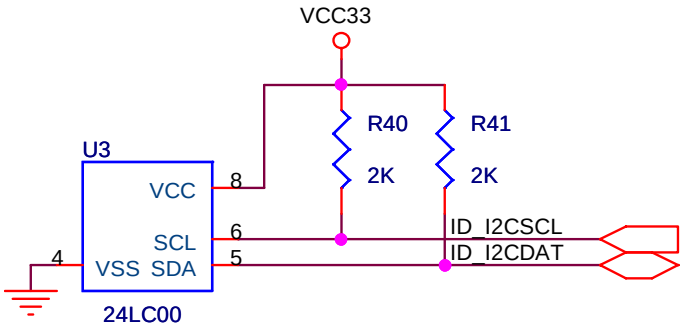

Figure 4.12. I2C Serial EEPROM schematic.

HSMC Connector		MAX II		I2C Serial EEPROM		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_ID_I2CSCL	41	T17	N3	ID_I2CSCL	6	EEPROM I2C Clock
HC_ID_I2CDAT	42	P18	P3	ID_I2CDAT	5	EEPROM I2C Data

Table 4.12. I2C Serial EEPROM pin assignments.

4.10 SD Card Interface

The MTDB includes a SD card socket and provides both SPI and SD 1-bit mode for SD Card access. Instructions for using SD card can be found by performing an appropriate search on various educational web sites. Figure 4.13 show the schematic of the SD card interface and the associated pin assignments are listed in Table 4.13.

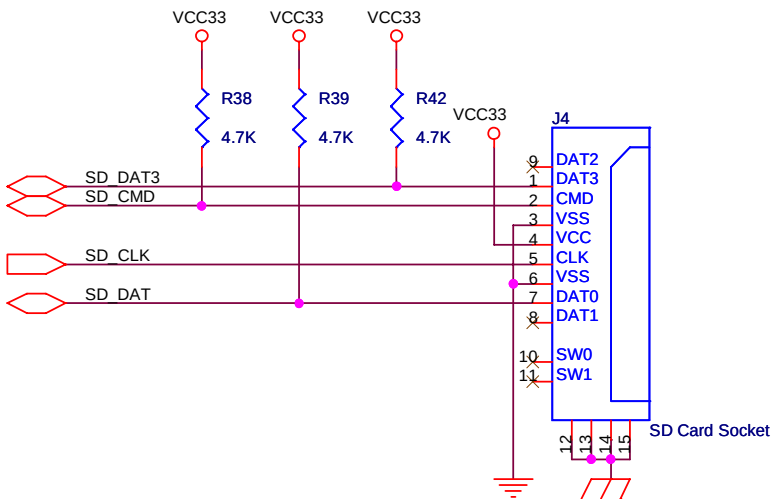

Figure 4.13. SD card interface schematic.

HSMC Connector		MAX II		SD Card		
Signal Name	Pin No.	HSMC Connector Side Pin	Device Side Pin	Signal Name	Pin No.	Description
HC_SD_DAT3	53	U11-2(*1)	U11-13(1)	SD_DAT3	1	SD 1-bit Mode: Card Detect; SPI Mode: Chip Select(Active Low)
HC_SD_CMD	44	U11-3(*1)	U11-12(1)	SD_CMD	2	SD 1-bit Mode: Command Line; SPI Mode: Data In
HC_SD_CLK	101	J16	P1	SD_CLK	5	Clock
HC_SD_DAT	48	U11-4 (*1)	U11-11(*1)	SD_DAT	7	SD 1-bit Mode: Data Line; SPI Mode: Data Out
Notes: (*1) These signals do not go through the MAX II chip. They pass through the MAX3378 level translator chip, U11.						

Table 4.13. SD card interface pin assignments.

Chapter 5
Examples of Advanced Demonstration

This chapter provides a few examples of advanced circuits implemented using MTDB and a Cyclone III Starter board. These circuits provide demonstrations of the major features on the board, such as its audio and video capabilities, and SD card connectivity. For each demonstration the Cyclone III FPGA configuration file is provided, as well as the full source code in Verilog HDL code. All of the associated files can be found in the *MTDB_demonstrations* folder from the **MTDB System CD-ROM**. For each demonstration described in the following sections, we give the name of the project directory for its files, which are subdirectories of the *MTDB_demonstrations* folder.

5.1 SD Card Music Player

Introduction

Many commercial media/audio players use a large external storage device, such as an SD card or CF card, to store music or video files. Such players may also include high-quality DAC devices to produce good audio quality. The Cyclone III Starter board and MTDB board provide the hardware and software needed for SD card access and professional audio performance so that it is possible to design advanced multimedia products using the Cyclone III Starter board and MTDB board.

Demonstration Operation

Refer to Figure 5.1 and 5.2. , follow the procedure below to operate the demonstration:

1. Make sure Quartus II 7.2 and Nios2 II EDS 7.2 are installed.
2. Connect Line-Out to a speaker or earphone.
3. Connect Cyclone III Starter board and host computer with an USB cable.
4. Power on the Cyclone III Starter board.
5. Execute the demo batch file “sdcard_audio.bat”. (*1)
6. Insert a SD card which has wave files located in the root folder. (*2)
7. Use BUTTON4 to select desired wave file and BUTTON3/BUTTON2 to adjust audio volume.(*3)

(*1) The batch file is located in the folder “MTDB_SD_Card_Audio\Demo Batch”

(*2) The SDCARD should be formatted as FAT16 and the wave file (*.WAV) must be stereo, 16-bits, 48K sample rate, and with short file name.

(*3) LED2 will be flashing when the SD card is not inserted in SD card socket. LED1 will be flashing while the demonstration is playing music.

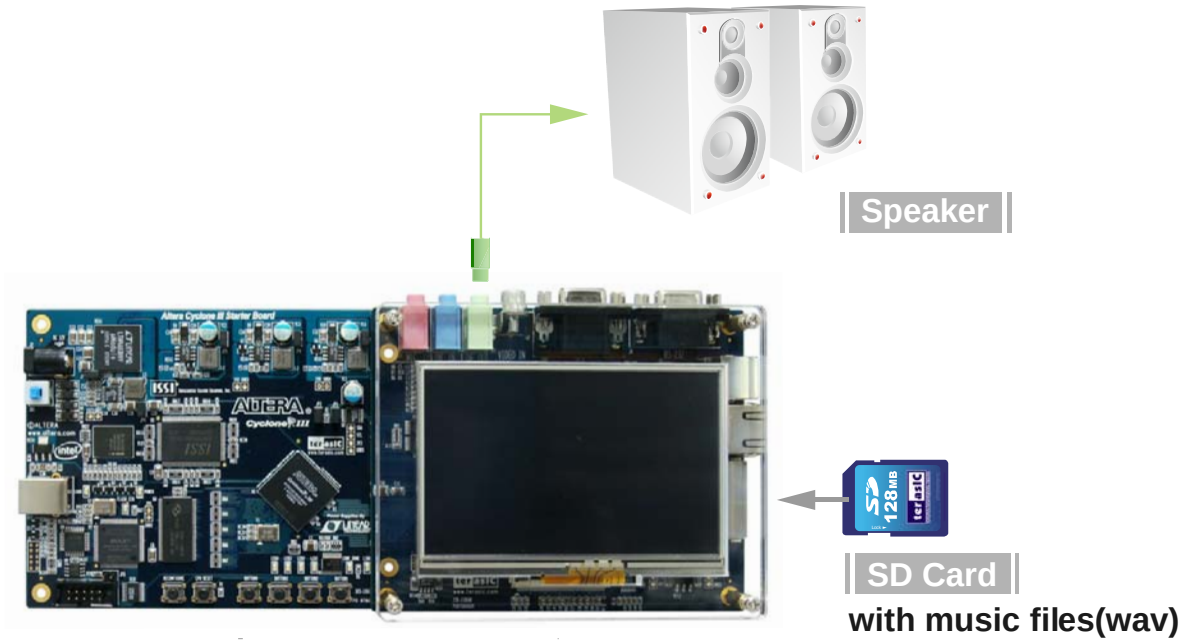

Figure 5.1. Setup of the SD Card Music Player Demonstration.

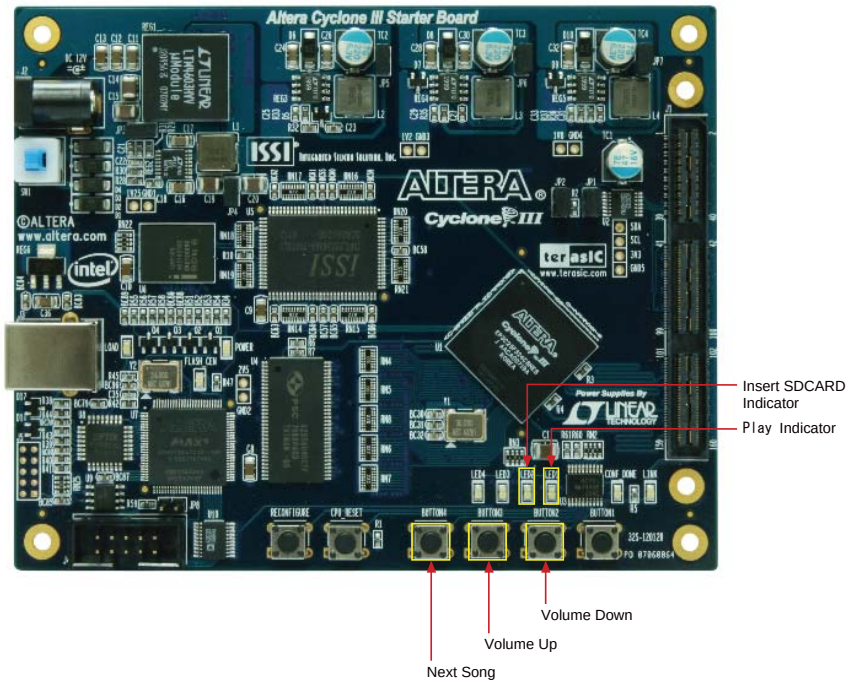

Figure 5.2. Man-Machine Interface of the SD Music Player Demonstration.

Source Code

■ Overview

All of the source codes in this demo program are included in the MPTD SYSTEM CD. The demo project is developed under Quartus II 7.2 and Nios II EDS 7.2. The Quartus project is located at the folder

"MTDB_Demonstration\MTDB_SD_Card_Audio",

and the NIOS II project is at:

"MTDB_Demonstration\MTDB_SD_Card_Audio\software".

The demonstration program includes both hardware and software parts. The hardware part is built by SOPC Builder and the software part is built by Nios II EDS.

■ Hardware

The hardware is built by SOPC builder. The hardware block diagram is shown in Figure 5.3. In this SOPC, a NIOS II processor is added to control the whole system. The NIOS II C program is stored in the SSRAM of the Cyclone III starter board. JTAG-UART is added for debug and shows prompt messages for this demonstration.

A user-defined SOPC component, called AUDIO_DAC_MATER, is provided for streaming audio signal data from NIOS II to the audio codec chip. There is a 16x256-byte DAC-FIFO in the controller to queue audio data for playing. This component directly interfaces the audio chip and communicates the audio chip with the three pins BCLK, DACDAT, and DACLRCK. Also, it provides the input crystal for the audio chip.

In this demonstration, the audio chip is configured as slave mode, so external circuitry must provide the ADC/DAC serial bit clock (*BCK*) and left/right channel clock (*LRCK*) to the audio CODEC. The sample rate is configured as 48K over-sampling, so a clock 18.432MHz (48K x 384) must be provided to the XTI/MCLK pin of the audio chip. The BYPASS mode of the audio chip is enabled, so line-out will mix the data from microphone-in and line-in for the Karaoke-style effects.

Two PIO pins are used to implement I2C protocol for configuring the audio codec chip. (For SDCARD,) Four PIO pins are used to implement 1-bit mode SD-MODE protocol for reading data from SD-CARD. Buttons and LEDs on the Cyclone III starter board are also controlled by the PIO controller.

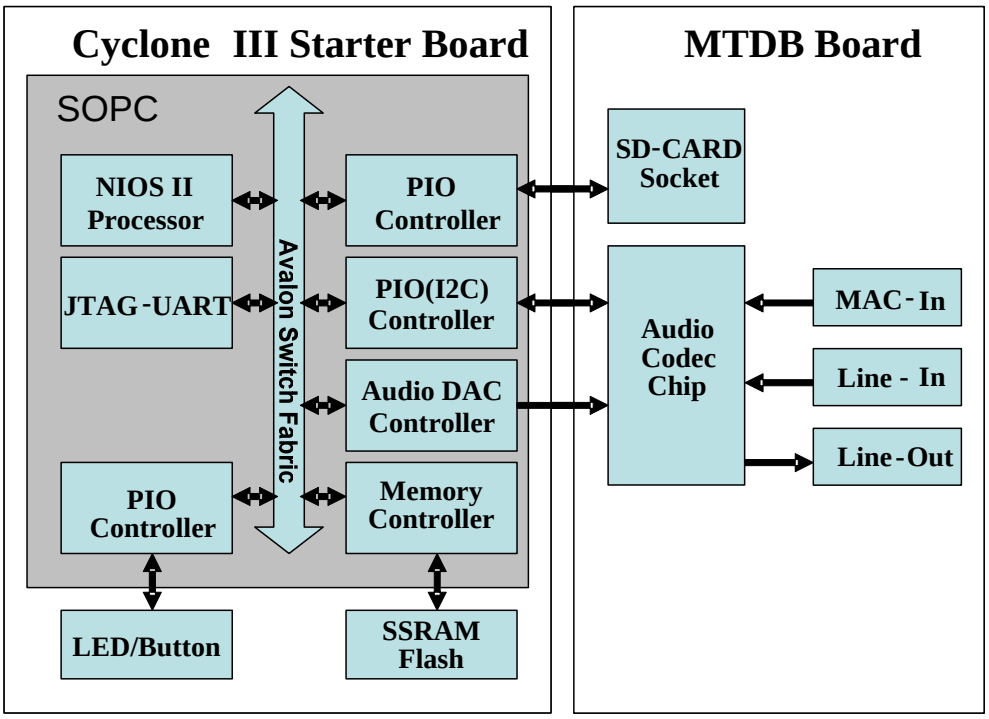

Figure 5.3. Hardware Block diagram of the SD card Music Player Demonstration.

■ Software

The software is implemented by C and the software architecture is shown in Figure 5.4. In the block diagram, the Audio DAC module provides functions to check whether DAC FIFO is full, and be in charge of sending audio data to the DAC FIFO. The I2C module implements the I2C protocol. The SDCARD module implements the 1-bits SD-MODE protocol. The FAT16 module implements FAT16 file system. In this module, only read function is implemented. The WAVE module implements WAVE file decode function. All access to Avalon bus is performed through the both fundamental system calls IOWR and IORD which are defined in <io.h>.

When the program starts, it configures the audio chip through I2C protocol. The audio chip is configured as:

- ✓ Slave Mode
- ✓ 48K Over-Sampling
- ✓ 16-bits, Left-Justified Format
- ✓ Enable BYPASS mode.

Then, it checks whether SDCARD is existed. If yes, it will build a play list by searching the root folder of the SD card and finding those wave files supported by this program. If the play list is not empty, it starts to play first wave file by reading audio signal data from SDCARD and sending the audio data to the audio chip. Each time, it reads 512 bytes audio data from SDCARD, and sends the data to DAC-FIFO if it is not full.

In the interval of streaming 512 bytes audio data, the main program polls the button status. If users press BUTTON3 or BUTTON2 to adjust audio volume, the main program will configure the audio chip volume through I2C protocol immediately. If users press BUTTON4 to select next song, it will close current wave file and open next wave file for new audio playing.

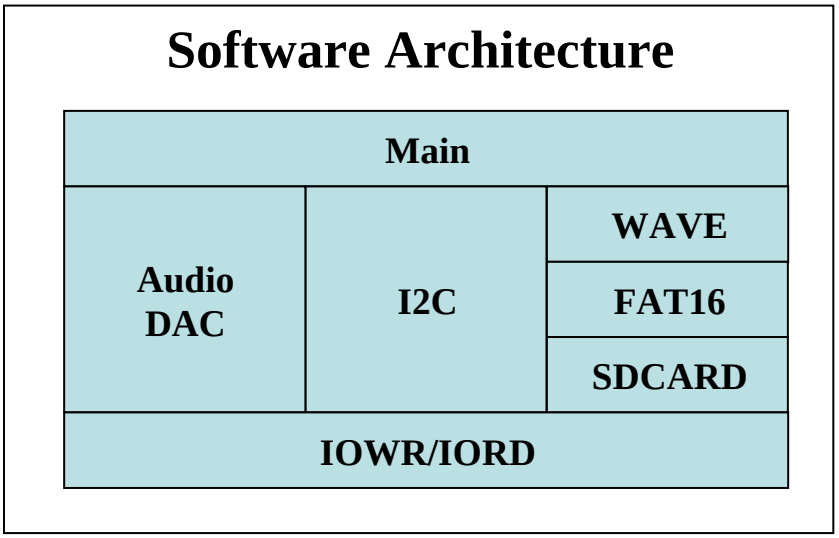

Figure 5.4. Software Block diagram of the SD Music Player Demonstration.

5.2 Music Synthesizer Demonstration

This demonstration shows how to implement a Multi-tone Electronic Keyboard using Cyclone III Starter board and MTDB board with a PS/2 Keyboard and a speaker.

PS/2 Keyboard is used as a piano keyboard for input. The FPGA on the Cyclone III Starter board serves as a Music Synthesizer to generate music and tones. The VGA connected to the MTDB board is used to display which key is pressed during the playing of the music.

Figure 5.5 shows the block diagram of the design of the Music Synthesizer. There are four major blocks in the circuit: *DEMO_SOUND*, *PS2_KEYBOARD*, *STAFF*, and *TONE_GENERATOR*. The *DEMO_SOUND* block stores a demo sound for user to play; *PS2_KEYBOARD* handles the users' input from PS/2 keyboard; The *STAFF* block draws the corresponding keyboard diagram on VGA monitor when key(s) on the PS/2 Keyboard are pressed. The *TONE_GENERATOR* is the core of music synthesizer.

User can switch the music source either from *PS2_KEYBOAD* or the *DEMO_SOUND* block using BUTTON2.

Figure 5.6 illustrates the setup for this demonstration.

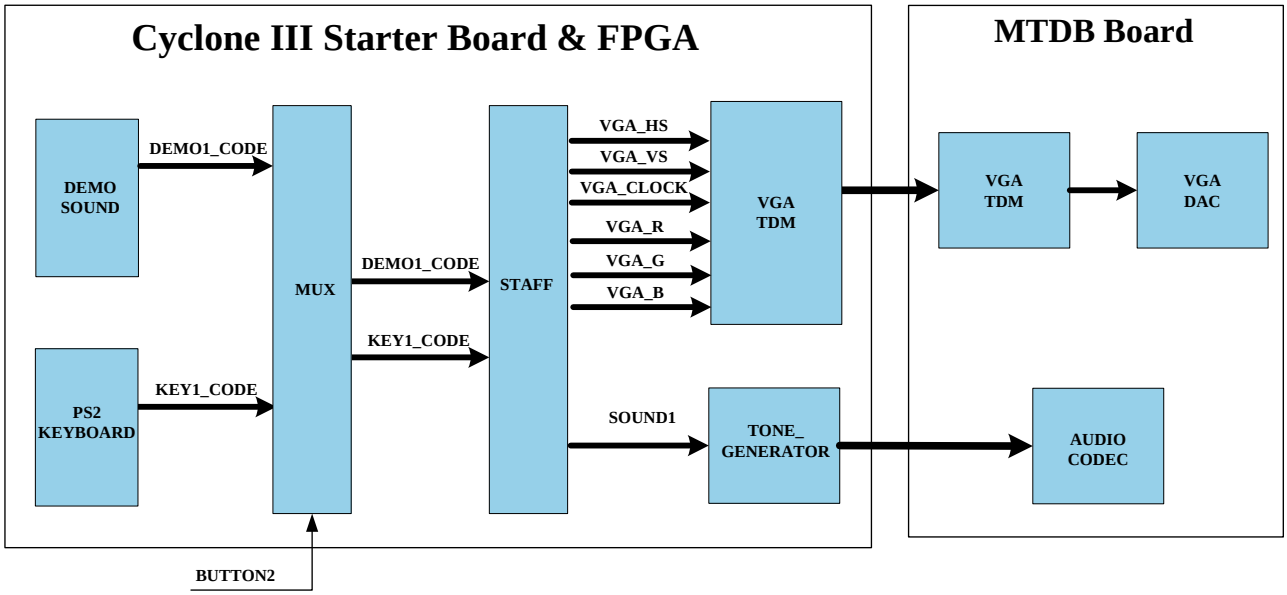

Figure 5.5. Block diagram of the Music Synthesizer design

Demonstration Setup, File Locations, and Instructions

- Project directory: *MTDB_Synthesizer*
- Bit stream used: *MTDB_Synthesizer.sof* or *MTDB_Synthesizer.pof*
- Connect a PS/2 Keyboard to the MTDB board.
- Connect the VGA output of the MTDB board to a VGA monitor.
- Connect the Line-out of the MTDB board to a speaker.
- Load the bit stream into FPGA on the Cyclone III Starter board.
- Press BUTTON[1] on the Cyclone III Starter board to reset the circuit
- Press BUTTON[2] on the Cyclone III Starter board to start the music demo

Table 5.1 and 5.2 illustrate the usage of the switches, pushbuttons (BUTTONs), and PS/2 Keyboard.

-
- Switches and Pushbuttons

Signal Name	Description
BUTTON [1]	Reset Circuit
BUTTON [2]	Press BUTTON [2]: Demo Music Mode. Release BUTTON [2]: PS2 Keyboard Mode.
BUTTON [4]	Reset Keyboard.

Table 5.1. Usage of the switches and pushbuttons (BUTTONs).

- PS/2 Keyboard

Signal Name	Description
Q	-#4
A	-5
W	-#5
S	-6
E	-#6
D	-7
F	1
T	#1
G	2
Y	#2
H	3
J	4
I	#4
K	5
O	#5
L	6
P	#6
:	7
“	+1

Table 5.2. Usage of the PS/2 Keyboard’s keys.

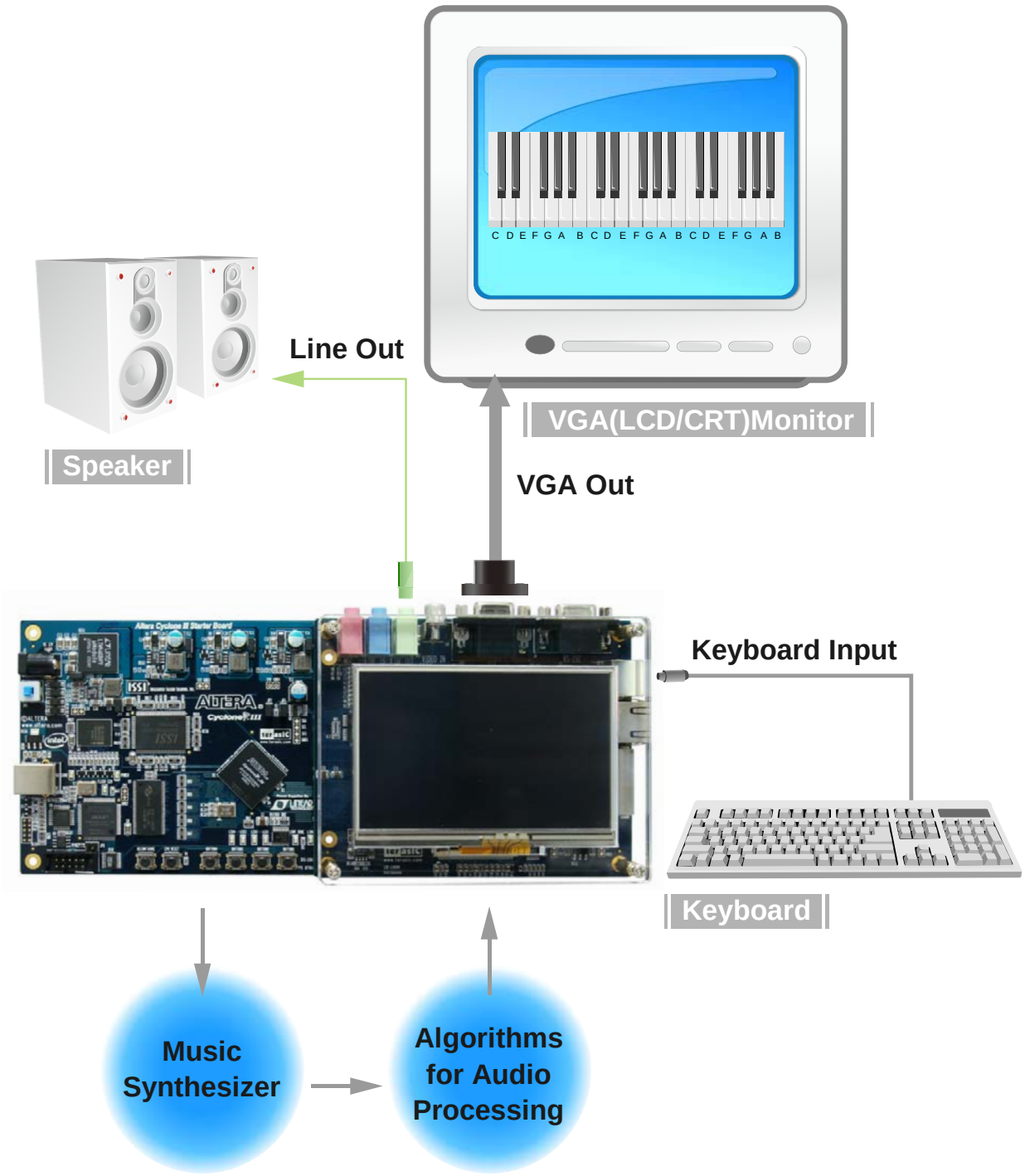

Figure 5.6. The Setup of the Music Synthesizer Demonstration.

5.3 LCD TV Demonstration

This demonstration plays video and audio input from a DVD player using the LCD Touch panel module, audio CODEC, and one TV decoder on the MTDB board. Figure 5.7 shows the block diagram of the design. There are two major blocks in the circuit, called *I2C_AV_Config* and *TV_to_VGA*. The *TV_to_VGA* block consists of *ITU-R 656 Decoder*, *SDRAM Frame Buffer*, *YUV422 to YUV444*, *YCrCb to RGB*, and *VGA Controller*.

As soon as the bit stream is downloaded into the FPGA on the Cyclone III starter board, the register values of the TV Decoder chip will be configured via the *I2C_AV_Config* block, which uses the I2C protocol to communicate with the TV Decoder chip on the MTDB board. Upon the power-on sequence, the TV Decoder chip will be unstable for a time period; the *Lock Detector* is responsible for detecting this instability.

The *ITU-R 656 Decoder* block extracts *YCrCb 4:2:2 (YUV 4:2:2)* video signals out of the *ITU-R 656* data stream , which is sent by the TV Decoder. It also generates a data valid control signal indicating the valid period of data output. Because the video signal from the TV Decoder is interlaced, we need to perform de-interlacing on the data source. We used *Frame Buffer* and a *field selection multiplexer(*MUX*)* which is controlled by the *LCD controller* to perform the de-interlacing operation. Internally, the *LCD Controller* generates data request and odd/even selected signals to the *Frame Buffer* and *filed selection multiplexer(*MUX*)*. The *YUV422 to YUV444* block converts the selected *YCrCb 4:2:2 (YUV 4:2:2)* video data to the *YCrCb 4:4:4 (YUV 4:4:4)* video data format.

The *YCrCb_to_RGB* block converts the *YCrCb* data into RGB output. The *LCD Timing Controller* block generates standard LCD sync signals *LCD_HD* and *LCD_VD* to the *LCD TDM block*. The *LCD TDM Controller* block will take these sync signals and RGB data as input and multiplex these signals to the MAXII CPLD device on the MTDB board via the HSMC connector.

Finally, the *LCD TDM Controller block* in the MAXII CPLD device will de-multiplex the LCD RGB data and the sync signals, before sending them to the LCD Touch panel module for display.

Figure 5.8 illustrates the setup for this demonstration.

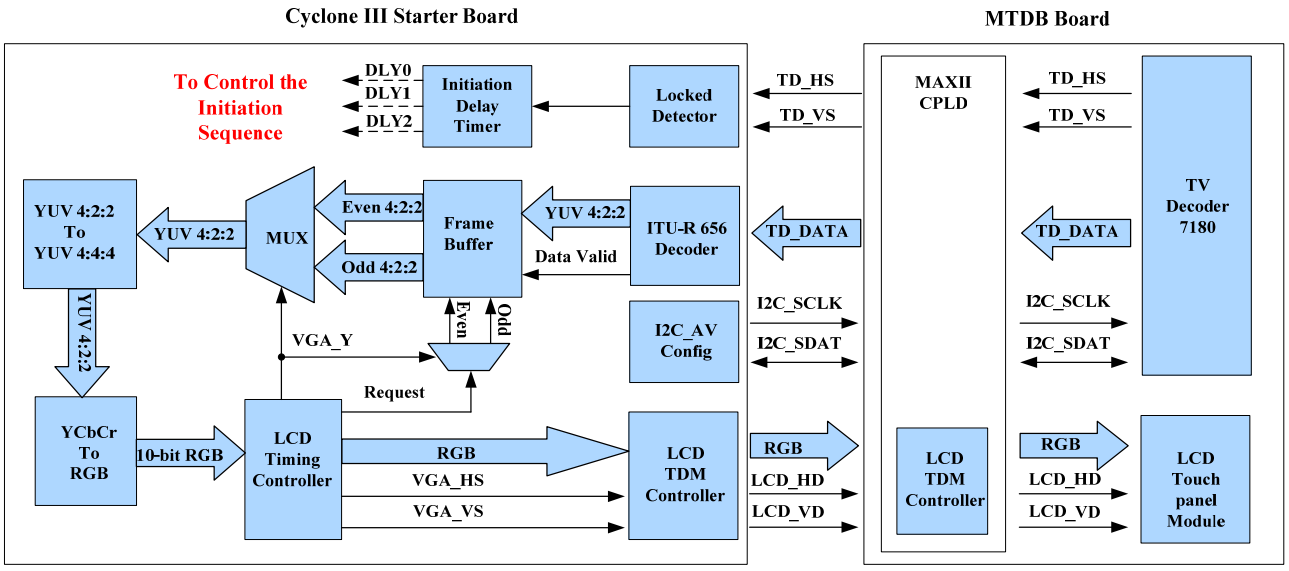

Figure 5.7. Block diagram of LCD TV design

Demonstration Setup, File Locations, and Instructions

- Project directory: *MTDB_LCD_TV*
- Bit stream used: *MTDB_LCD_TV.sof* or *MTDB_LCD_TV.pof*
- Connect a DVD player's composite video output (yellow plug) to the **Video-IN** RCA jack (J11) of the MTDB board. The DVD player has to be configured to provide
  - NTSC output
  - 60 Hz refresh rate
  - 4:3 aspect ratio
- Connect the audio output of the DVD player to the line-in port of the MTDB board and connect a speaker to the line-out port. If the audio output jacks from the DVD player are of RCA type, then an adaptor will be needed to convert to the mini-stereo plug supported on the MTDB board; this is the same type of plug supported on most computers
- Load the bit stream into FPGA on the Cyclone III Starter board.
- Press BUTTON1 on the MTDB board to reset the circuit.

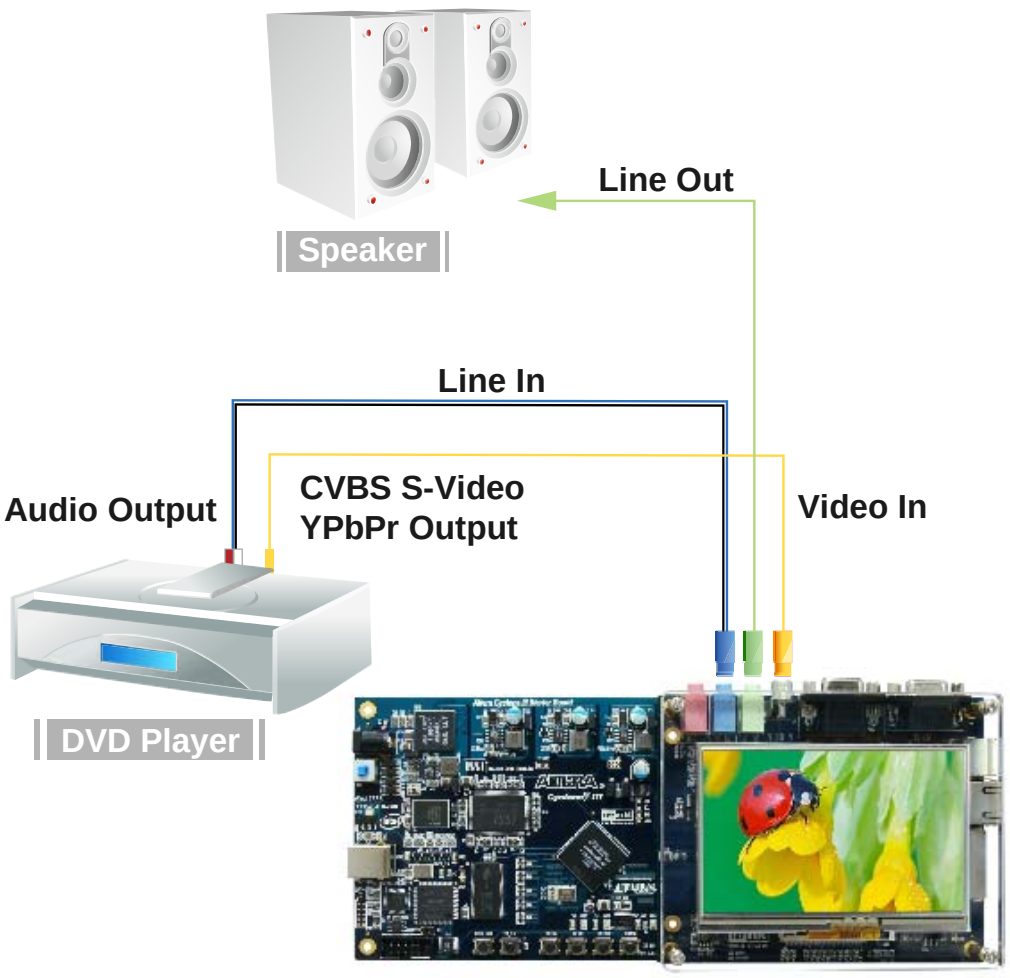

Figure 5.8. The setup for the LCD TV demonstration.

Chapter 6
Appendix

6.1 Revision History

Version	Date	Change Log
V1.0	2007.11.28	Initial Version (Preliminary)